ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 4, April 2014

Voltage Unbalance Elimination in Multilevel Inverter using Coupled Inductor and Feedback Control

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ABSTRACT: This paper deals with the voltage unbalance problem in multilevel inverters. Multilevel voltage source converters are the new trend in the power converter option for high-power applications. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The elimination of voltage unbalance in a single-phase five-level inverter which uses coupled inductors and feedback control, which can produce a five level output voltage with only one dc source. With this topology, splitting of the dc voltage is avoided, which eliminates the problem of voltage balancing in the circuit which was a prominent problem in the conventional topologies. The feedback control of the inverter is implemented using a PI controller. The six power switches used here have the same voltage stress and only one set of coupled inductors are adopted.

KEYWORDS: Multilevel inverter, PI controller, Coupled inductor, Power switches, Voltage unbalance.

I.INTRODUCTION

Multilevel converters are becoming an enabling technology in many industrial sectors. Multilevel converters have been under research and development for more than three decades and have found successful industrial application [1]-[5]. However, this is still a technology under development, and many new contributions and new commercial topologies have been reported in the last few years. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels in these types of inverters normally involve voltage clamping or capacitor charge control. These topologies use multiple dc voltage sources and multiple dc voltage capacitors [7], [8]. This is a great challenge when it comes to volume, weight, and cost minimization. The main problem with them is mainly the balancing of the dc capacitor voltages. The various applications of multilevel inverters: motor drives, active filters, power conditioning, energy storage in renewable energy systems, fuel cell energy systems, hybrid electric vehicles (HEV).

In all multilevel topologies with several DC link, the voltage balancing problem of DC capacitors was the key problem. The chopper circuit were used for DC capacitor voltage balancing in diode clamped multilevel inverters.[16] The most important are the topologies like diode clamped inverter, capacitor clamped, and cascaded multicell with separate DC source and the emerging topologies were asymmetric hybrid cells and soft switched multilevel inverters. The most relevant control and modulation methods developed for the family of converters are: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space vector modulation. [15] The most desirable topology is a multilevel inverter with only one dc source and no split capacitors but unfortunately this type of inverter has yet to be discovered .The voltage unbalance is a problem which reduces the efficiency of the output voltage in multilevel inverters [6],[9],[10]. The development of a multilevel inverter with better control unit will eliminate the problem of voltage unbalance. A single-phase five-level inverter using coupled inductors is studied in this paper. With the proposed inverter, only one dc voltage source is needed and split of the dc voltage capacitor is also avoided, which eliminates the problem of dc capacitor voltage balancing with the conventional topologies. Six power switches with the same voltage stress and only one set of coupled inductors are adopted [11]. It is, in fact, the adoption of the coupled inductors that makes it possible to generate an output of five-level voltage with only one dc voltage source. The presented topology is very suitable for low to medium power applications and also for high-current cases.

In an open loop system the errors in the output are not rectified automatically. The use of a closed loop system helps to attain a better quality output with improved control features. A pi controller unit is chosen in order to realize the closed

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loop configuration [13]. The voltage and current outputs from the proposed inverter are fed back to the controller. The pi controller processes its available data, compares it with the preset reference value and calculates the deviation from the ideal working condition [14],[15]. The rectification is made by the controller by the switching pattern control and firing control of the switching elements used in the inverter topology. Thus an improved output waveform with reduced distortion and better controllability with reduced number of switches and with no voltage unbalance problem is obtained.

II. SINGLE PHASE MULTILEVEL INVERTER WITH COUPLED INDUCTORS AND FEEDBACK CONTROL

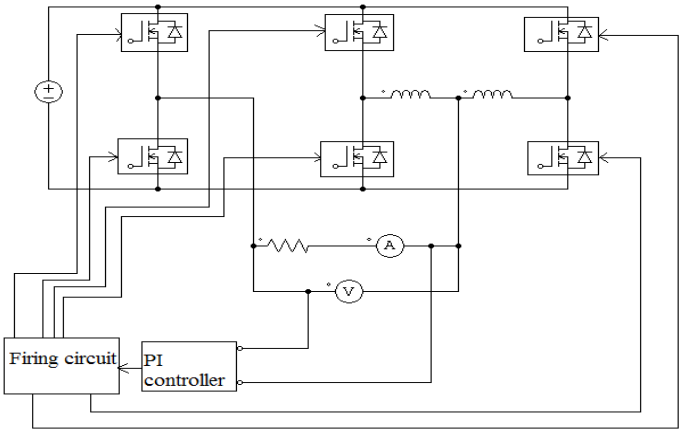

Figure 1: Proposed Single-Phase five-Level Inverter.

The figure 1 represents the circuit diagram of the inverter using coupled inductors. 2E is the dc input voltage and L_1 and L_2 are the two coupled inductors. The mutual inductance of the two inductors is M and the output terminals of this inverter are 1 and 2. Obviously, this topology is very simple and can be constructed simply by the addition of a coupled inductor to a conventional three-arm inverter bridge. It is the adoption of the coupled inductors that makes it possible to output five-level voltage with only one dc voltage source. Suppose that the two coupled inductors are with the same number of turns or obtained by a center-tapped inductor.

The leakage inductances of the two inductors are Lσ1 and Lσ2, respectively. Assuming that $L_{\sigma 1} = L_{\sigma 2} = L_\sigma$, the voltage equations of the coupled inductors can be expressed as follows:

$$(M+L_\sigma)\frac{di_b}{dt} - \left(M\frac{di_c}{dt}\right) = v_{bn} - v_{2n} \quad (1)$$

$$(M + L_\sigma) - \left(M\frac{di_b}{dt}\right) = v_{cn} - v_{2n} \quad (2)$$

Meanwhile, according to Kirchhoff's current law, one can obtain

$$i_b + i_c + i_l = 0 \quad (3)$$

From (1) to (3), the following equation can be derived:

$$v_{2n} = \frac{v_{bn}+v_{cn}+L_\sigma\frac{di_l}{dt}}{2} \quad (4)$$

Generally, the leakage inductance can be designed to be very small and its influence can be ignored in most cases. Therefore, (4) can be rewritten as

$$v_{2n} = \frac{v_{bn}+v_{cn}}{2} \quad (5)$$

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This result is interesting and shows that the coupled inductors will perform as an adder of the two input voltage at the non-common-connected terminals with the common-connected terminal as the output. Actually, without the help of the coupled inductors, the proposed inverter will not be able to output five-level voltage. The power switches in one arm are assumed to switch complementarily. For instance, S_2must be turned OFF if S_1 is turned ON and vice versa.

So the following discussion will only focus on the switching states of the switches S_1, S_5, and S_3. For convenience of analysis, the number "1" will be used to denote the ON state of one switch and "0" will be used to denote the OFF state. In fact V_{1n}, V_{bn}, and V_{cn} all can generate two-level voltage (+E and −E). According to (6), the voltage levels of V_{12} can be summarized in Table 3.1. The proposed inverter can generate five voltage levels at its output terminals. From Table 3.1, it should be pointed out that the switching state of S_1 must be 1 if $V_{12} \geq 0$ and the switching state of S_1 must be 0 if $V_{12} \leq 0$. This means $S_1$and S_2 will switch at the fundamental frequency of the reference signal. So, the switching losses of S_1 and S_2 will be very low in the proposed inverter. The output voltage of the proposed inverter can be expressed as

$$v_{12} = v_{1n} - v_{2n} = v_{1n} - \frac{v_{bn}+v_{cn}}{2} \tag{6}$$

Table 1: Switching States and Output Voltage of Inverter

S_1	S_3	S_5	V_{12}
1	0	0	+E
1	0	1	+E/2
1	1	0	+E/2
0	0	0	0
0	0	1	-E/2
0	1	0	-E/2
0	1	1	-E

III. DESIGN OF THE COUPLED INDUCTORS

In order to design the coupled inductors, the relationship between the currents of the coupled inductors i_b, i_c and the load current i_l should be analyzed. Using (1) and (2) and neglecting the leakage inductance, one can obtain

$$\frac{2M\,di_b}{dt-2M} \times \frac{di_c}{dt} = V_{bc} \tag{7}$$

Solving (3) and (9), the currents in the coupled inductors can be expressed as follows

$$i_b = \frac{1}{2}\left(-i_l + i_{ripple}\right) \tag{8}$$

$$i_c = \frac{1}{2}\left(-i_l - i_{ripple}\right) \tag{9}$$

Where

$$i_{ripple} = \frac{1}{2M}\int v_{bc}\,dt \tag{10}$$

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Suppose the ripple current in the coupled inductors is limited to ΔI, the inductance M can be determined. Considering the most serious condition, i.e., $|v_{bc}|$ is always equal to 2E within one Ts, the largest ripple current in the coupled inductors can be calculated as follows:

$$i_{ripple(max)} = \Delta I = \frac{1}{2M}\int_0^{T_s} 2E\,dt = \frac{T_s \times E}{M} \quad (11)$$

Hence, the inductance M should satisfy

$$M > \frac{T_s \times E}{\Delta I} \quad (12)$$

The coupled inductors also carry half the load current besides the ripple current. It is clear from (11) that one inductor and thus the switch S_3/S_4 carries about half the load current if the ripple component is low. The high-switching frequency devices (S_3, S_6) take only half the load current while the low-switching frequency devices (S_1, S_2) carry the whole load current. Thereby, the switching and conduction losses of S_3, S_6 will not be very high because they only carry half of the load current. This characteristic of the proposed inverter makes it very suitable for high-current applications.

IV.FEEDBACK CONTROL

The first arm of the circuit is given gating signals using pulse generator. The next two arms which have the coupled inductor is the main part of the circuit. Actually, without the help of the coupled inductors, the proposed inverter will not be able to output five-level voltage. So the feedback control is provided only to the last two arms. The output voltage and current are used to realize the closed loop control. This is done using the pi controller and comparator unit. Thus by implementing a closed loop control, the output voltage quality is improved and it remains steady for any type of load condition. Since there is no use of dc link capacitors in this circuit, the problem of voltage unbalance is eliminated. The gating signals are given to the MOSFETS in the second and third arm by comparing the output voltage wave with a triangular wave. From the fourier analysis of the circuit it can be shown that the THD decreases. The voltage unbalance in the circuit is eliminated.

The proposed single-phase five-level inverter is based on coupled inductors. This inverter can output five-level voltage with only one dc source and no split of the dc voltage capacitor, totally avoiding the voltage balancing problem. The height of the staircase in the output voltage is only half of the dc-link voltage under any modulation index. Meanwhile, the voltage stresses on all the power switches are the same and only four switches are operated at high frequency. It is, in fact, the adoption of the coupled inductors that make it possible to output five-level voltage with only one dc voltage source. No split of the dc voltage capacitor is needed, totally avoiding the voltage balancing problem in conventional multilevel inverters. Six power switches with the same voltage stress and only one set of coupled inductors are adopted. This inverter is based on the widely used three-arm power module and the voltage stresses on all the power switches are the same, making it very easy to construct. The presented topology is very suitable for low to medium power applications, especially for high-current cases.

V. RESULT AND DISCUSSION

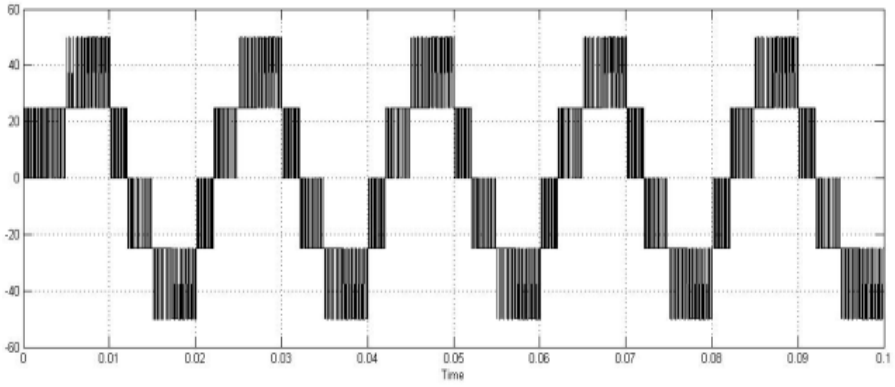

Fig. 1 Output Voltage Waveform

The output of the multilevel inverter presented here is a five level voltage. The output voltage is taken across the load

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connected across the common and non common terminal. The absence of voltage unbalance in the output voltage is visible from the output voltage waveform. The presence of coupled inductor is the main element responsible for the generation of five level output voltage using just six switches. This output voltage is taken as the feedback signal to the PI controller. The output waveform for 100V DC input is given above. A five stage output is obtained. The voltage levels are 100V, 50V, 0V, -50V, -100V. These levels are shown in the graph above.
The current through the load arm is measured. The output current waveform is obtained by connecting a current source in series with the load. The current is in the range of milli amperes. The value of the current is 0.025mA. The current ripples are absent and it is clear from the output waveform. This current waveform is also fed to the PI controller as feedback signal. The PI controller unit processes the voltage and current waveforms to generate the firing pulses.

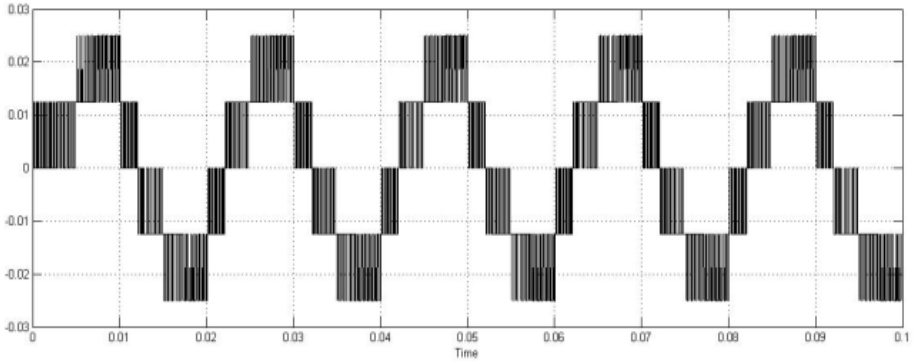

Fig. 2 Output Current Waveform

The firing pulses as given to the MOSFETS in the order of s1, s2, s3, s4, s5 and s6 are given in the graph shown above. The firing pulses for the first arm are given using pulse generators and the firing pulses to the other arms are given using feedback.

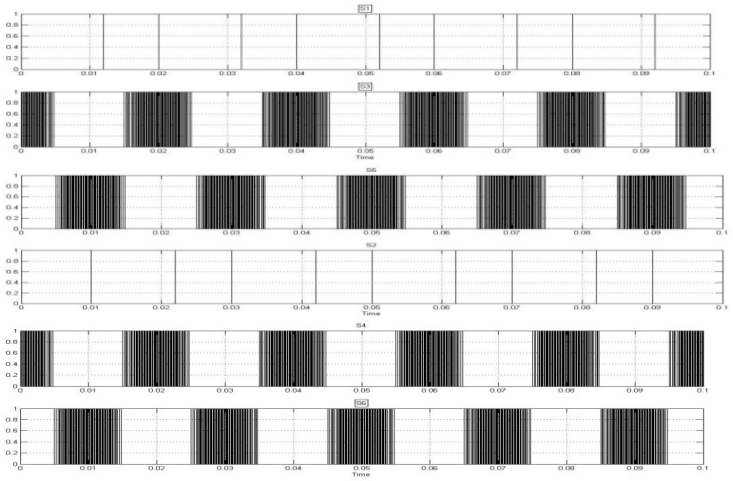

Fig. 3 Firing Pulses

The firing pulses are generated by comparing the output of the PI controller with the triangular wave. This process is done inside the subsystem. The switches in the first arm are provided with the firing pulses using pulse generators. The switches in the other two arms are given firing pulse by the comparison of the output of the PI controller with a triangular wave; this process is done inside the subsystem.

VI. CONCLUSION

The proposed single-phase five-level inverter is based on coupled inductors and closed loop configuration. This inverter

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can output five-level voltage with only one dc source and no split of the dc voltage capacitor, totally avoiding the voltage balancing problem. The FFT analysis of the proposed circuit in the closed loop conditions shows the THD values of the system.

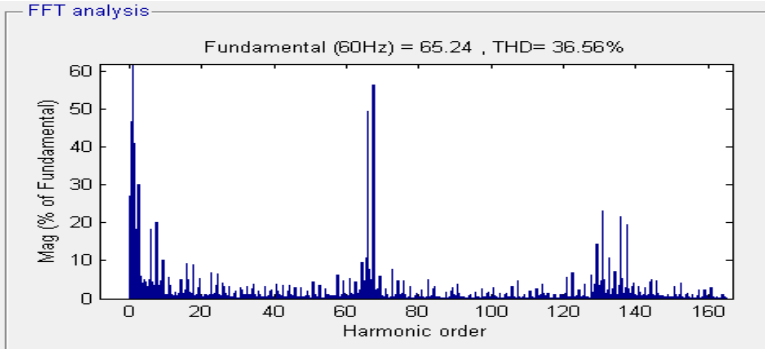

Fig. 4 FFT Analysis

The closed loop control in the proposed system uses both the voltage and current feedback. From the FFT analysis the THD value of the circuit has been obtained as 36.56 % and hence it is proven that the proposed system is more efficient. Verification of the results show validity of the proposed topology and the feedback control.

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