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Current Mode Computational Circuits for Analog Signal Processing

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ABSTRACT: The paper presents current adder and subtractor circuits based on cascode current mirror with improved linearity and wide linear range. The proposed circuits can be used for analog signal processing applications such as amplifiers, operational transconductance amplifiers (OTA), Gm-C filters, etc. In the proposed circuits, cascode current mirror topology is employed to improve current mirroring operation. The proposed circuits have been simulated using TSMC 0.18µm CMOS process technology with a supply voltage of 1.8 V. The proposed circuits operate efficiently within the current range of 0 to 80µA with the permissible error percentage of less than 2.5%. The SPICE simulation results have been presented to demonstrate the effectiveness of the proposed circuits.

KEYWORDS: Adaptive biasing, cascode current mirror, current mode circuits, adder, subtractor..

I.INTRODUCTION

In low-voltage/ low-power analog systems, current-mode signal processing has been usually considered an attractive strategy due to its potential for high-speed operation and low-voltage compatibility [1]-[4]. The behaviour of electrical circuits is always the result of interplay between voltage and current. In current mode circuits (CMCs), the currents determine the complete circuit response. The voltage signals are irrelevant in determining the circuit performance. Current-mode circuit (CMC) techniques which process the active signals in the current domain have simple architectures. The CMCs are suitable for integration in CMOS technology as they do not require specially processed capacitors or resistors and hence, they are more compatible with digital CMOS technology making integration of mixed signal circuits more feasible. In a current mode circuit, a change in current level is not necessarily accompanied by a change in the voltage level. Hence, the parasitic capacitances do not affect the operating speed of the circuit by a significant amount [5]. Therefore many conventional voltage mode circuit topologies have been replaced by new and innovative current mode designs because current mode approach proves a better alternative for low voltage high performance analog circuitdesign in which the circuit designer is more concerned with current levels for the operation of the circuits.

II. BACKGROUD

The current mirrors (CMs) are one of the basic building blocks of current mode circuits which are used in analog signal processing cells [3], [6]-[10]. These are used as biasing structures or constant current sources and as an active load in amplifier stages since, it offer high impedance [11]-[12]. It is used to generate a replica of given reference current. It can also amplify or attenuate the reference current. Ideally, the output impedance of a current source/ sink should be infinite and capable of generating or drawing a constant current over a wide range of voltages. However, the finite value of output resistance and a limited output voltage required to keep device in saturation ultimately limits the performance of the current mirror [13]-[16]. Current mirror topology based analog circuits have simple structures and leads to easy implementation of operations such as addition and subtraction.

Several authors have proposed current mode computational circuits in literature [17-19]. Ferri et al. [17] have proposed simple current mirror based current subtractor. In [18], a current subtractor using PMOS wide swing cascode current mirror has been suggested. Lin et al. [19] have proposed current subtractor based on flipped voltage follower cell.
In this paper, we have proposed current mode computational circuits such as current subtractor and current adder based on NMOS cascode current mirror (CCM) topology with improved linearity.

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The paper is organized as follows: In Section II, the principles and architectures of the proposed current subtractor and adder based on CCM topology is described. The simulation results are presented in section III. The paper is concluded in section IV.

III. PROPOSED CURRENT ADDER AND CURRENT SUBTRACTOR CIRCUITS BASED ON NMOS CASCODE CURRENT MIRROR

Current mirrors are one of the most important and widely used building blocks of analog architectures. Conventional current mirrors operate on the principle that if the gate-source voltage of the two identical MOS transistors is equal, then the drain currents should be equal [13]. The conventional current mirror is shown in Figure 1.

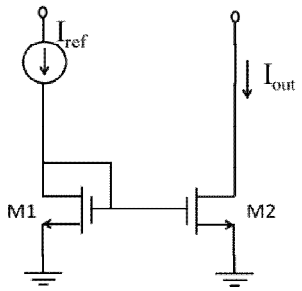

Figure 1: Conventional current mirror [13]

The drain currents I_{D1} and I_{D2} of transistors M1 and M2, respectively, are given as

$$I_{D1} = \frac{1}{2}\mu_n C_{ox} (W/L)_1 (V_{GS1} - V_{TH})^2(1 + \lambda V_{DS1}) \quad (1)$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox} (W/L)_2 (V_{GS2} - V_{TH})^2(1 + \lambda V_{DS1}) \quad (2)$$

where μ_n is the charge-carrier effective mobility, C_{ox} is the gate-oxide capacitance per unit area, $(W/L)_1$,$(W/L)_2$ are aspect ratios, V_{GS1},V_{GS2} are gate-source voltages, V_{TH} is threshold voltage, V_{DS1},V_{DS2} are drain-source voltages and λ is the channel length modulation parameter of transistors M1 and M2, respectively.

Since, the transistor M1 is diode connected, the drain-source voltage of transistor M1 (V_{DS1})is equal to its gate-source voltage (V_{GS1}).Also, gate terminals of both the transistors M1 and M2 are tied together, therefore gate-source voltages of M1 and M2 are equal (i.e.V_{GS1}=V_{GS2}). Using equations (1) and (2), the ratio of drain currents I_{D1} and I_{D2} is given as

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\frac{(1+\lambda V_{DS1})}{(1+\lambda V_{DS2})} \quad (3)$$

Since, $V_{DS\ 1} \neq V_{DS2,}$ the drain currents of transistors M1 and M2 are not equal. Also, the effect of channel length modulation introduces the significant error in copying currents. To remove the drawback of channel length modulation effect in conventional current mirror, the idea of cascode structure is employed. Ability to suppress the channel length modulation effects in cascode current mirror (CCM) is achieved by making drain to source voltage of M1 and M2equal, so that output current (I_{out}) always follows the reference current (I_{ref}). In addition to this, cascode structure

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increases output resistance to $g_m r_o^2$, where g_m is the transconductance of the transistor. For implementing cascode current mirror structure, a cascode current source using NMOS transistor M3 is used, as shown in Figure 2.

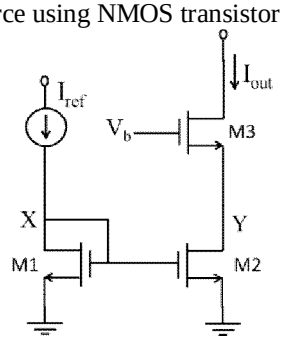

Figure 2: Cascode current source [13]

The bias voltage (V_b) of transistor M3 is chosen such that, voltage at node X (V_X) is equal to voltage at node Y (V_Y). By applying KVL in the loop consisting transistors M3 and M2 to ground, considering their respective gate voltages and voltage at node Y w.r.t ground, the voltage V_Y is given as

$$V_Y = V_b - V_{GS3} \text{ or } V_b = V_{GS3} + V_Y \quad (4)$$

From equation (4) it can be seen that if gate- source voltage is added to voltage at node X (V_X), then the required value of V_b can be obtained. Hence, another diode connected device M4 is placed in series with M1 as shown in Figure 3, thereby generating a voltage at node N (V_N) which is given as

$$V_N = V_{GS4} + V_X \quad (5)$$

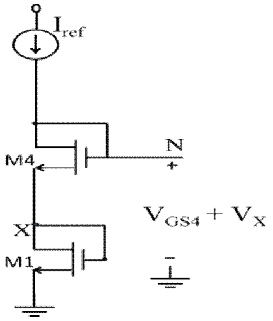

Figure 3: Modification of mirror circuit to generate the cascode bias voltage [13]

Connecting node N to the gate of transistor M3, as shown in Figure 4, the voltage at node N is given as,

$$V_{GS4} + V_X = V_{GS3} + V_Y \quad (6)$$

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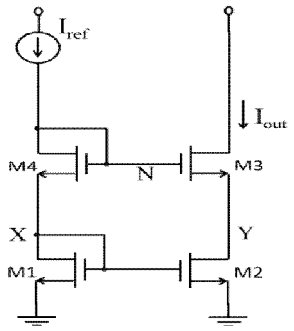

Figure 4: Cascode current mirror [13]

From equation (6), it is observed that for V_X to be equal to be equal to V_Y, V_{GS3} and V_{GS4} has to be equal.

The ratio of drain currents of transistors M1, M2 and M3, M4 are given as

$$\frac{I_{D3}}{I_{D4}} = \frac{I_{D2}}{I_{D1}} \tag{7}$$

Since V_{GS1}= V_{GS2}, equation (7) is modified as

$$\frac{(W/L)_3(V_{GS3}-V_{TH})^2}{(W/L)_4(V_{GS4}-V_{TH})^2} = \frac{(W/L)_2}{(W/L)_1} \tag{8}$$

Now equation (8) reduces to

$$V_{GS3} = V_{GS4} \quad \text{if} \quad \frac{(W/L)_3}{(W/L)_4} = \frac{(W/L)_2}{(W/L)_1} \tag{9}$$

Using equations (6) and (9), the voltage V_Y is given as

$$V_Y = V_X \tag{10}$$

Hence, the drain currents of transistors M1and M2 become equal (i.e. $I_{D2} = I_{D1}$ or $I_{out} = I_{ref}$).

III(A) Proposed Current Adder Circuit based on CCM

The proposed current adder using NMOS type cascode current mirror is shown in Figure 5. All the transistors are biased in saturation region and the transistors M1-M2, M3-M4, M5-6, and M7-M8 are perfectly matched. The cascode current mirrors are developed using transistors M1-M4 and M5-M8 whose function is to precisely copy the input currents AI_{in1} and AI_{in2}, in transistor M4 and M8, respectively.

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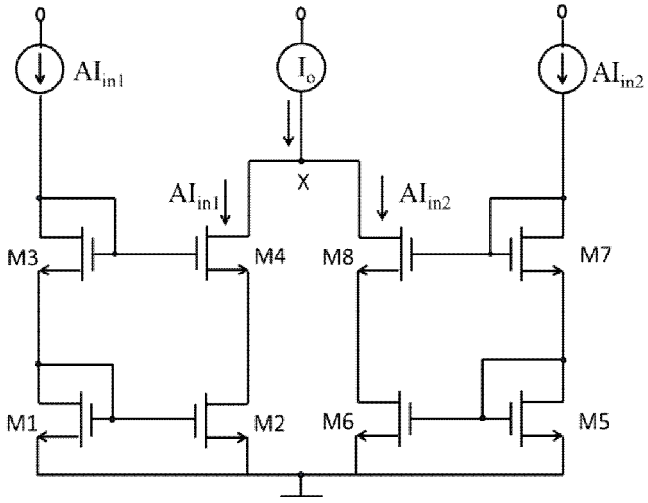

Figure 5: Proposed Current Adder based on CCM

The current $AI_{in1}$and $A_{in2}$is copied in transistors M2,M4 and M8,M9 by cascode current mirrors formed by transistors M1-M4 and M5-M8.For achieving the proper biasing voltage of cascode structure, the aspect ratios of transistors are chosen as,

$$\frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_2}{(W/L)_1}, \qquad \frac{(W/L)_7}{(W/L)_8} = \frac{(W/L)_5}{(W/L)_6} \tag{11}$$

Applying KCL at node X, the output current I_o is given as

$$I_o = A\, I_{in1} + AI_{in2} = A\,(I_{in1} + I_{in2}) \tag{12}$$

From equation (12), it can be seen that the output current is the addition of two input currents AI_{in1} and AI_{in2}, where A is the gain factor.

III(B) Proposed Current Subtractor Circuit based on CCM

Using the same topology of CCM, the current subtractor is also proposed which is shown in Figure 6. The cascode current mirrors are implemented by using NMOS transistors as active elements. All the transistors are biased in saturation mode and the transistors pairs M1-M2, M3-M4, M5-6, and M7-M8 are perfectly matched. The transistors M1-M4 and M5-M8 are arranged in cascode current mirror topology in which transistors pairs M1, M3 and M6, M8 are configured as diode connected to operate them in saturation region.

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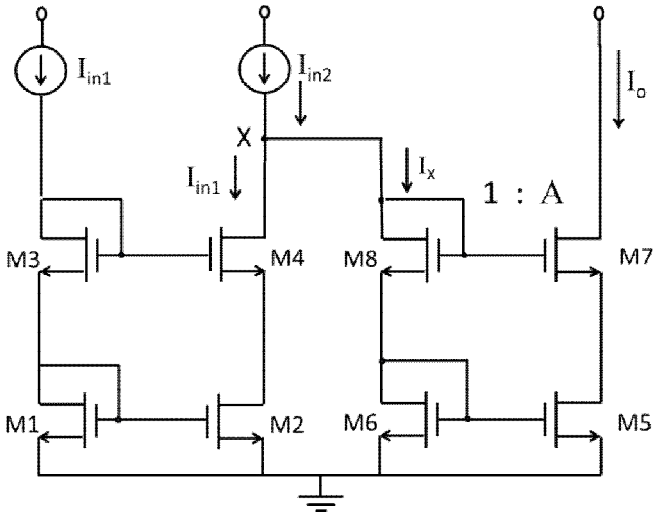

Figure 6: Proposed Current Subtractor based on CCM

The current I_{in1} is copied in transistors M2 and M4 by the cascode current mirror formed by transistors M1-M4.Another cascode current mirror is formed by transistors M5-M8 which mirrors the output current i.e. the subtraction of two currents. For the proper biasing voltage of cascode structure the aspect ratio of transistors are chosen as,

$$\frac{(W/L)_4}{(W/L)_3} = \frac{(W/L)_2}{(W/L)_1}, \qquad \frac{(W/L)_7}{(W/L)_8} = \frac{(W/L)_5}{(W/L)_6} \tag{13}$$

From Figure 6, it can be seen that current I_{in1} through transistors M1, M3 is copied accurately in transistors M2, M4 (i.e. I (M4, M2) = I_{in1}).

By applying KCL at node X, the current I_X is given as

$$I_X = I_{in2} - I_{in1} \tag{14}$$

Therefore, the output current I_o is given as

$$I_o = AI_X = A\,(I_{in2} - I_{in1}) \tag{15}$$

From equation (15), it can be seen that the output current is the subtraction of two input currents AI_1 and AI_2, where A is the gain factor. The proposed current subtractor circuit find wide application in adaptive biasing of amplifiers.

IV.SIMULATION RESULTS AND DISCUSSION

The proposed circuits have been simulated in TSMC 0.18µm CMOS process technology. The proposed computational circuits have been designed to operate within the current range of 0 to 80µA. The DC characteristics of the proposed current adder (Figure 5) is shown in Figure 7, in which output current varies from 10 µA to 90 µA w.r.t input current variation from 0 µA to 80µA and keeping one of the current sources fixed at 10 µA.Table I shows the comparison of theoretical and simulated values of output current. From the Table I, it can be seen that the percentage error between theoretical and simulated output current is less the 0.025%.

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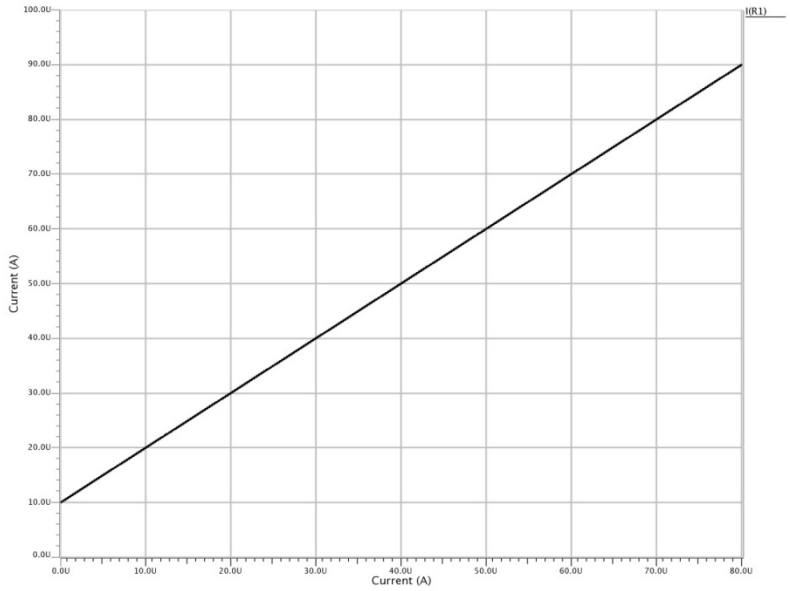

Figure 7: DC characteristics of proposed current adder circuit

From Figure7 it can be observed that the proposed current adder circuit shows good linearity response over a wide range of current. The improved linearity characteristics are attributed to the use of cascode current mirror topology which provides precise copying of the currents by eliminating the channel length modulation effect in conventional current mirrors. Table I shows the comparison of theoretical and simulated values of output current.

Table I: Comparison of theoretical and simulated values of output current of proposed current adder circuit

Input Current I_{in1}(µA)	*Input Current* I_{in2}(µA)	*Output Current* I_o(µA) ***(Theoretical Values)***	*Output Current* I_o(µA) ***(Simulated Values)***	*Percentage Error (%)*
0	10	10	10.002	0.020
10	10	20	20.005	0.025
20	10	30	30.005	0.016
30	10	40	40.004	0.010
40	10	50	50.001	0.002
50	10	60	59.998	0.003
60	10	70	69.994	0.008
70	10	80	79.988	0.015

The DC characteristics of current subtractor (Figure 6) is shown in Figure 8 ,in which output current varies from 80 µA to 0 µA w.r.t input current variation from 0 µA to 80 µA and keeping one of current sources fixed at 80 µA. Table IIshows the comparison of theoretical and simulated values of output current. From Table II, it can be seen that the % error in theoretical and simulated output current is less the 2.50%

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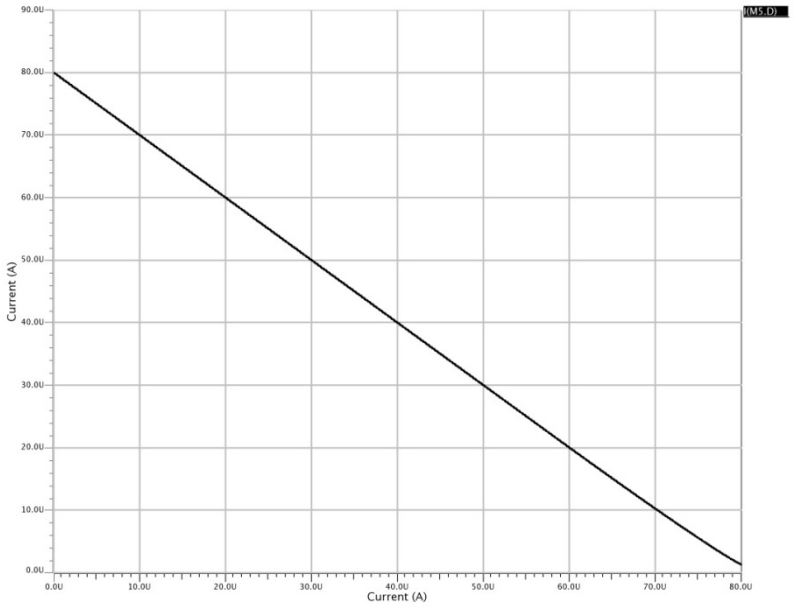

Figure 8: DC characteristics of proposed current subtractor circuit

From Figure 8 , it can be observed that DC characteristics of the proposed current subtractor are linear over appreciable range of input current, hence the subtraction of two currents at the output is achieved with good accuracy. Thus the current subtractor designed with cascode current mirror topology can be employed in adaptive biasing of amplifiers. Table II shows the comparison of theoretical and simulated values of output current, one of the input current is fixed to a value while the other current source is varied and output current is subtraction of the two input currents.

Table II: Comparison of theoretical and simulated values of output current in proposed current subtractor circuit

Input Current I_{in1}(µA)	*Input Current* I_{in2}(µA)	*Output Current* I_o(µA) ***(Theoretical Values)***	*Output Current* I_o(µA) ***(Simulated Values)***	*Percentage Error (%)*
0	80	80	80.000	0.000
10	80	70	69.994	0.008
20	80	60	59.994	0.010
30	80	50	49.996	0.008
40	80	40	40.000	0.000
50	80	30	30.006	0.020
60	80	20	20.030	0.150
70	80	10	10.250	2.500

IV.CONCLUSION

The proposed computational circuits for addition and subtraction operation have been developed using TSMC 0.18µm CMOS process technology. The proposed current subtractor and adder circuits have wide operating range of current of 0 to 80µA. The SPICE simulation results show that the proposed circuits have a good linearity response over a wide

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range of current. These circuits are useful for various analog signal processing applications such asamplifiers, operational transconductance amplifiers (OTA), Gm-C filters,etc.

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