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Reversible Multiplier – A Review

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ABSTRACT: Increasing demand for reduction in power dissipation in digital computer system has led to new mode of computation for digital design giving birth to reversible computing. Its main aim is low power dissipation in logical elements but can have some other advantages likeerror preventionand data security. In present-day, reversible logic has bring out to be an optimistic computing model having applications in low power CMOS, nanotechnology, quantum computing and DNA computing. This paper presents reviews about various purposed schemes used to designn×nreversible multiplier. The reversible multipliers are optimized in terms of total quantum cost, number of ancillary inputs, number of garbageoutputs and hardware complexity.

KEYWORDS: Reversible logic gate, Reversible logic circuit, Reversible multiplier, Quantum computing, Nanotechnology.

I. INTRODUCTION

The usual general- purpose computing system is logically irreversible unavoidably generate heat. The inputs are not generalized from the outputs in irreversible logic.During any computation the intermediate bits used to compute the final results are erased. Hence, information loss causes energy dissipation in computing system was demonstrated by R.Landauer in the year 1960. According to Landauer's[1] principle, a computer must dissipate atleast kTIn2 of energy (about 3×10^{-21} J at room temperature) for each bit of information is erased, where k = $1.3806505\times10^{-23}m^2kg^{-2}K^{-1}$ is Boltzman constant and T =273.16 K is absolute temperature. Gordon. E. Moore [2] in 1965 predicted that the number of transistors onto a chip will double after every 18 months. According to Moore's law as the number of components on the chip increases the power dissipation also increases rapidly. Hence power dissipation has become an important issue in integrated circuits.In 1973, C.Bennett [3] ,revealed that the reversible logic circuits would not loose kTIn2 joules of energy as outputs can be recovered from inputs.Bennett showed that the computations that are performed on classical machine can be performed with the same efficiency with less power dissipation on the reversible machine. The research on the reversibility was started in 1980's based on Bennett's concept.Shor[4]in 1994 did a remarkable research work in creating an algorithm using reversibility for factorizing large numbers with better efficiency than the classical computing theory. After his work on reversible computing has been started in different fields such as quantum computing, low power CMOS design and nanotechnology.

II.RELATED WORK

Because of extensive use of multipliers in computer system, several reversible circuits for implementing multipliers have been purposed. Reversible multiplier is a computingdevice, used to multiply two binary numbers by the use of reversible adders. The basic multiplication process involves computing a set of partial products, and then summing the partial products together.

In 2008, Haghparast et al.[5] have introduced a reversible multiplier structure.The design uses an array of 16 Peres gates for the generation of partial products and then addition of partial products is accomplished by adder designed with combination of Peres gate and HNG gate. In the same year, Shams et al.[6] purposed the similar design with the Peres gates for the partial product generation and MKG for the addition at final stage of multiplication.

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In year 2010, a new design for reversible 4×4 multiplier is purposed by H.R. Bhagyalakshmi et al.[7]It consists of three sections for multiplication; additional is fan-out circuit along with partial product generator and additional circuits. In year 2012, M..Z. Moghadamet al.[8] purposed two approaches to design the ultra- area- efficient multiplier, in which partial product generation is carried out with Peres and Toffoli gates respectively. The number of garbage outputs are reduced when partial products are generated with Peres gate and Toffoli gate.

III.REVERSIBLE GATES

A reversible logic gate is an n-input, n-output device with one-to-one mapping[3], which helps to retrieve the inputs from the outputs and vice-versa. The main challenges for the reversible logic are reducing the power dissipation, reducing number of gates, delay and quantum cost.

1.The Reversible logic:

The n-input and k-output Boolean function f(a_1,a_2,a_3…a_n) is called reversible function if :

i. Mapping is one-to-one between input vector and output vector.
ii. The number of inputs is equal to number of outputs.
iii. Fan-out and feedback are not permitted.

2.Basic Definitions Related To Reversible Logic:

(i)Quantum Cost: The Quantum Cost refers to the cost of the circuit in terms of the cost of primitive gates (number of gates composed the circuit). The quantum cost of NOT gate (1×1) is 0 and that of any 2×2 gate (CNOT or Feynman gate) is 1.[11]

(ii) Constant Inputs / Ancillary Inputs: Ancillary/constant inputs can be defined as the inputs to be retained at constant value of '0' or '1' in order to generate the given logical function.[9]

(iii)Garbage Outputs: The garbage outputs are additional outputs in the reversible logic circuit that maintain the reversibility logic but do not perform any useful operation [10].The following formula shows relation between Garbage Output and Ancillary Inputs:

Input (n) + Constant/Ancillary Input = Output (k) + Garbage Output.

(iv)Total Logical calculations: The total logical calculation [10] is another term in reversible logical circuits, which indicates the XORs, NOTs and ANDs .Total Logical calculations are represents by the (L).Hereα =number of XORs,β =number of ANDs andδ =number of NOT gates.

3.Basic Reversible Logic Gates:

An n-input and n-output function f_n is said to be reversible if and only if there is a one-to-one [2]correspondence between the inputs and the outputs. An N×N reversible logic gate can be represents as follow:

$$I_{vector} = (I_1, I_2, I_3 \ldots\ldots I_n)$$
$$O_{vector} = (O_1, O_2, O_3 \ldots O_n)$$

Where I_{vector} and O_{vector} are input and output vectors respectively.In reversible logic gates, number of inputs(n) are equal to number of outputs(n).In this section we review the Reversible logic gates.

(i)Feynman Gate: Feynman gate is 2×2 reversible gates[11], called as CNOT (Controlled NOT) gate. It is widely used as fan-out purposes.Quantum cost for Feynman gate is 2.The total logical calculations of this gate is; T= 1α.

Fig.1.Symbol of Feynman gate and its quantum representation

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The input and outputvectors of 2×2 Feynman gate are as follows:
I_{vector}= (A, B)
O_{vector}= (X= A, Y= A⊕ B)

(ii)Toffoli Gate: ToffoliGate is also called as CCNOT (Controlled Controlled NOT) gate is a 3×3 reversible gate[12]. TG is a universal reversible gate.If the target input (C) is set to '0',then the gate will perform AND operation. Quantum Cost for Toffoli gate is 5. The total logical calculations of this gate are; T= 1α+1β.

Fig.3.Symbol of Toffoli gate and its quantum representation

The input and output vectors of 3× 3 Toffoli gate is:
I_{vector}= (A,B,C)
O_{vector}= (X=A, Y=B, Z=AB⊕C)

(iii)Peres Gate: Peres gate is a new 3×3 Toffoligate[13]. Quantum Cost for Peres gate is 4. Due to less quantum cost, it is used to implement several logic functions. Peres gate can be used as half adder, and a two-input AND gate. The total logical calculations for Peres gate are (T)= 2 α+1β.

Fig.4.Symbol of Peres gate and its quantum representation

The input and output vector of 3× 3 Peres gate:
I_{vector} =(A,B,C)
O_{vector}= (X=A, Y=A⊕B, Z=AB⊕C).

(iv)HNG Gate:HNG is 4×4 reversible gates. HNG can singly work as reversible full adder [5]. Thus QC of HNG full adder is minimum possible QC for a full adder design. (QC= 6). The total logical calculations for TSG gate is 5α + 2β.

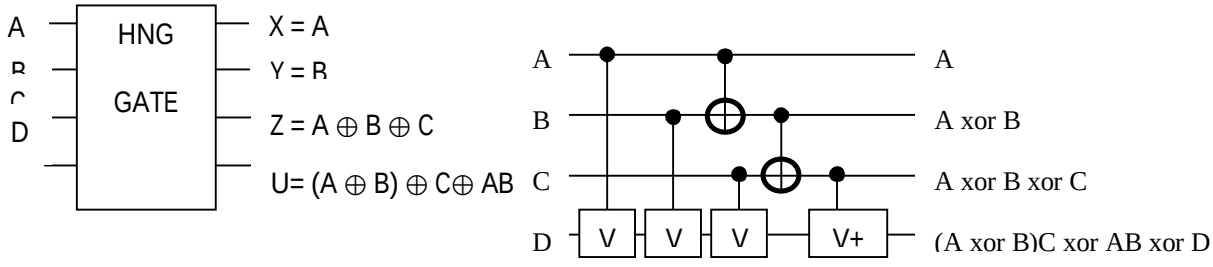

Fig.7.Symbol for HNG and its quantum representation.

The inputs and outputs vectors of HNG gate are as follows:
I_{vector}= (A, B, C,D)

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O_{vector}= (X=A, Y=B, Z=A⊕B⊕C, U= (A⊕B).C⊕AB⊕D)

(v)TSG Gate:TSG is a 4×4 reversible gate. The TSG gate is capable of implementing all Boolean functions and can also work as reversible full adder[15]. The total logical calculations for TSG gate are 6α + 3β + 3δ.

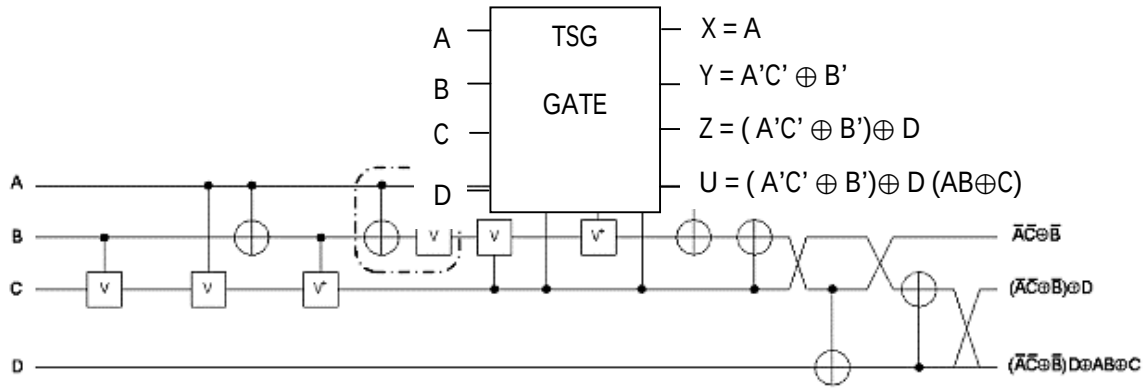

Fig.8.Symbol for TSG and its quantum realization.

The inputs and outputs vector of TSG gate are as follows:
I_{vector}= (A,B,C,D)
O_{vector}= (X=A, Y=A'C'⊕ B')
Z=(A'C'⊕B') D
U= (A'C'⊕B') ⊕ D (AB⊕ C)

(vi)MKG Gate:MKG is 4×4 reversible logic. It can also singly work as a reversible full adder.[5]. Qunatum cost for MKG gate is 13. The total logical calculations for MKG gate are 5α + 3β + 3δ.

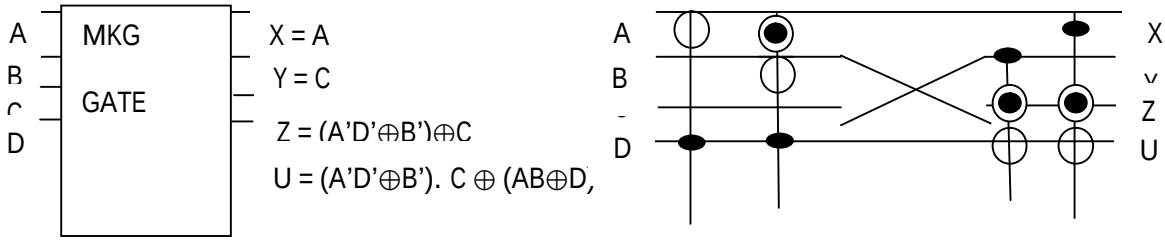

Fig.8.Symbol for MKG and its quantum realization.

The inputs and outputs vectors of MKG gate are as follows:
I_{vector}= (A, B, C,D)
O_{vector}= (X=A, Y=C, Z=(A'D'⊕B') ⊕C, U= (A'D'⊕B').C ⊕ (AB⊕D)

IV.QUANTUM COMPUTING THEORY

Quantum gate are defined based on quantum computing theory. Quantum gates act on small units of quantum data, called qubits (Quantum bits). The qubit state (q) is superposition of 0 and 1 state, is denoted by $|1\rangle$ and $|0\rangle$, respectively [16] . The qubit state represents as:

$$q = \alpha |0\rangle + \beta |1\rangle \quad \text{(i)}$$

where α and β are two complex numbers and $|\alpha|^2 + |\beta|^2 = 1$.

When the complex numbers α = 1 and β = 0, the case corresponds to the binary state '0'. Similarly when the complex numbers α = 0 and β = 1, the case responds to the binary '1'. All the combinations of α and β are not basis binary (0 or 1).So, a qubit is described by two dimensional vectors, represents as[17]:

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$$\begin{pmatrix}\alpha\\ \beta\end{pmatrix} \text{or} \begin{pmatrix}u_0\\ u_1\end{pmatrix} = \begin{pmatrix}0\\ 1\end{pmatrix} \quad \text{(ii)}$$

The effect of quantum gates on quantum state can be explained by vector operations , where the quantum gates are represented by unitary matrix.A generalized 2- qubit controlled U gate [17] is shown in fig. 9. Its Unitary matrix is represents asfollows:

$$\text{Controlled U} = \begin{pmatrix}1 & 0 & 0 & 0\\ 0 & 1 & 0 & 0\\ 0 & 0 & u_{11} & u_{12}\\ 0 & 0 & u_{21} & u_{22}\end{pmatrix}$$

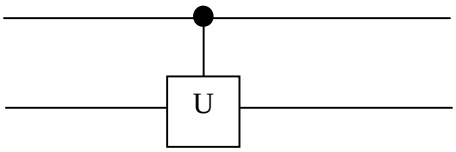

Fig.9. Controlled U gate

Two well known quantum gates are V and V^+[17].The gate V, named as square root of NOT or Controlled NOT gate. In Controlled-V gate, when the controlled input (A) is '0', the data output remains same as its data input B. But the data output becomes V(input) when the controlled input becomes '1'.

$$\text{V}=\begin{bmatrix}0 & 1\\ 1 & 0\end{bmatrix}^{1/2} = \frac{1+i}{2}\begin{bmatrix}1 & -i\\ -i & 1\end{bmatrix} \text{(iii)}$$

$V^+$is the Harmition of Controlled V gate matrix. Similar rules apply to V^+, except that its data outputs becomes V^+ (input) when the controlled input (A) is '1'.

$$V^+ = \frac{1-i}{2}\begin{bmatrix}1 & i\\ i & 1\end{bmatrix} \text{(iv)}$$

The properties of V and V^+ gates are given as follows:

$$V \times V^+ = \text{NOT} \quad \text{(v)}$$

$$V^+ \times V^+ = \text{V} \times \text{V} = \text{I} = \begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix} \text{(vi)}$$

V.DIGITAL MULTIPLIER

Reversible multiplier is a digital circuit, used to multiply two or more binary numbers. Multiplication is laboriously used arithmetic operations in many computational units. It is necessary for a processor to have high speed multiplier. So, now a day reversible multipliers are in demand. The basic cell for multiplier is a full adder .The multiplier design has two segments which work sequentially:

Segment 1: Partial Product generation

Segment 2: Addition of Partial Products generated in segment 1.The operation of 4×4 multiplier is depicted in fig.8.

$$\begin{array}{lllll} & & & & x_3x_2x_1x_0\\ \times\ y_3 & y_2 & y_1 & y_0 & \\ \hline & & & x_3y_0 & x_2y_0 \quad x_1y_0 \quad x_0y_0\\ & & x_3y_1 & x_2y_1 & x_1y_1 \quad x_0y_1\\ & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2\\ \text{carry} & x_3y_2 & x_1y_2 & x_1y_2 & x_1y_2\\ \hline P7 & P6 & P5 & P4 & P3\ P2 \quad P1 \quad P0 \end{array}$$

Fig.8. Partial products in 4×4 multiplication.

1.**Partial Product Generator**:Partial product of an n×n multiplier requires n×n 2-input AND operation. 2-input AND operations can be realized by using reversible gates. As it is not permissible to have a fan-out of a gate, so we have to use reversible gate to produce replications of signals.

2.Addition of partial products : Addition of partial products can be done by any of the digital adder according to the circuit requirement. Reversible gates adders are used for addition purpose. Full adder and half adders can also be in use if the computations are for small values. For designing n×n multiplier, we need n(n-2) full adder and n half adders.Different adders along with the different parameters are shown in the table:

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Comparison Study of various reversible multipliers:

Multiplier	Quantum Cost	No. of Ancillary inputs	No. of Garbage outputs	No.of gates	Total Cost
M.Z.Moghadam,K.Navi (Design I) [8]	136	36	28	32	196
M.Z.Moghadam,K.Navi (Design II) [8]	144	28	24	28	196
Haghparast et al.[5]	140	28	28	28	196
Bhagyalakshmiand venkatesha [7]	152	52	52	40	244
Haghparast et al.[6]	152	52	52	52	256
Islam et.al [21]	144	28	52	52	290
Banerjee and pathak [20]	168	76	50	80	298
Thapliyal and Srinivas [19]	234	58	58	53	345

In 2006,Thapliyal and Srinivas [19] proposed a reversible multiplier, using TSG gates. Total quantum cost for multiplier was 345. Many researchers then after proposed multiplier using different reversible gates.Quantum cost further reduced to 244 by a new improved design purposed by H.R. Bhagyalakshmi [5] in 2010. In year 2012, a design is purposed by M.Z.Moghadam et al. This design reduces the quantum cost to 196 by the use of TG [12] and PG[13] gates for the partial product generation.

VI.APPLICATIONS

Reversible computing is used in areas which require high energy efficiency, speed and performance. It includes the areas like:

- Design of low power arithmetic and data path for digital signal processing (DSP) .
- Low power CMOS design.
- DNA Computing
- Quantum Computer
- Computer Graphics
- Nanotechnology
- FPGA in CMOS Design

VII.CONCLUSION

Reversible multiplier can be designed with the different logical designs purposed in conventional combinational and sequential logic with the aim to improve the performance of computational units. To improve the performance, the main measures in designing an efficient reversible logic multiplier are: Number of gates, Number of garbage outputs, Number of ancillary inputs, total quantum cost and total logical calculations.

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