ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 8, August 2014

Low Power Area-Efficient Adiabatic Vedic Multiplier

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ABSTRACT: In this paper, we describe adiabatic Vedic multiplier using efficient charge recovery logic (ECRL). Today Power dissipation minimization is the basic principle in making any electronic product portable. Even though there has been a decrease in circuit operating voltages, significant power is lost in switching elements (transistors). With adiabatic logic most of the energy is restored to the source instead of dissipating as heat. Proposed work focuses on the design of low power and area-efficient adiabatic Vedic multiplier using TSMC0.18µm CMOS process technology In Tanner Tool v13.

Keywords*:* adiabatic, low power, area-efficient, Vedic multiplier.

I. INTRODUCATION

Design of Adiabatic Vedic multiplier using EEAL (Energy Efficient Adiabatic Logic) is proposed in literature [1].In this paper, we described low power area-efficient Adiabatic Vedic multiplier using ECRL (Efficient Charge Recovery Logic). The multiplier architecture is based on Urdhava-triyakbhyam sutra or vertical and crosswise multiplication algorithm of antique Indian Vedic mathematics. Adiabatic 8x8 Vedic multiplier is designed using Tanner Tool v.13.

Adiabatic is the term taken from thermodynamic means no heat exchange with the environment. Instead of dissipating as heat during discharge period energy is mostly restored as supply. With conventional CMOS technology half of energy is required for charging capacitor and remaining half of the energy dissipated as heat during discharge period. In this approach slow charging of capacitor by using ac power supply and partial recovery of energy by slowly decreasing supply. In this paper ECRL (efficient charge recovery logic) has been proposed to achieve low power and area-efficient based on DCVS logic style. With, ECRL logic number of transistors utilization is reduced by using of single DCVS network with that energy consumption is also less.

The rest of this paper is organized as follows. Section II describes the previous work. Section III describes about ECRL inverter with reduced number of transistors using proposed logic. Section IV shows the general implementation of NxN Vedic multiplier based on the Urdhava - Tiryakbhyam sutra or "vertical and crosswise "algorithm and Implementation of EEAL and ECRL adiabatic 8x8 multiplier. Section V describes experimental results and comparison of the number of transistors used and power dissipation of our logic with other logic style described. Finally, conclusions are given in section VI.

II. RELATED WORK

EEAL is a dual rail adiabatic logic, which consists of two DCVS network and a pair of cross-coupled PMOS devices in each stage, as shown in figure 1 (a).

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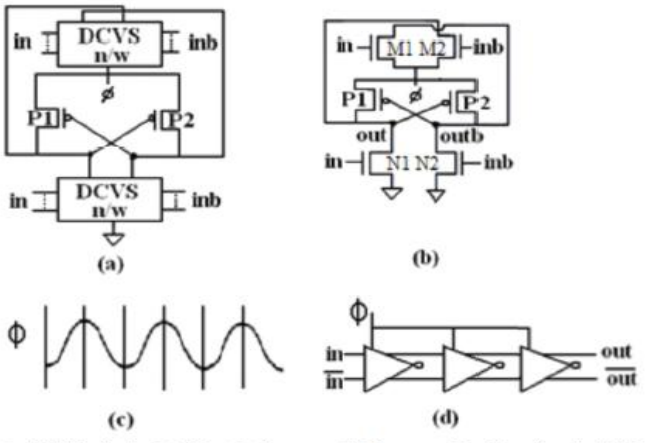

Fig.1 (a) EEAL LOGIC block diagram (b) Inverter/Buffer circuit (c) Power supply (d) cascading of inverter/buffer circuit

In Fig 1 two DCVS network are used for fast charging of the capacitor. But the number of transistor utilization is doubled, which leads to high power consumption. We proposed logic for low power and area efficient to do Vedic multiplication

III. PROPOSED LOGIC

ECRL (Efficient Charge Recovery Logic) is a dual rail adiabatic logic, which consists of a single DCVS network and a pair of cross coupled PMOS devices in each stage, as shown in fig 2 (a).

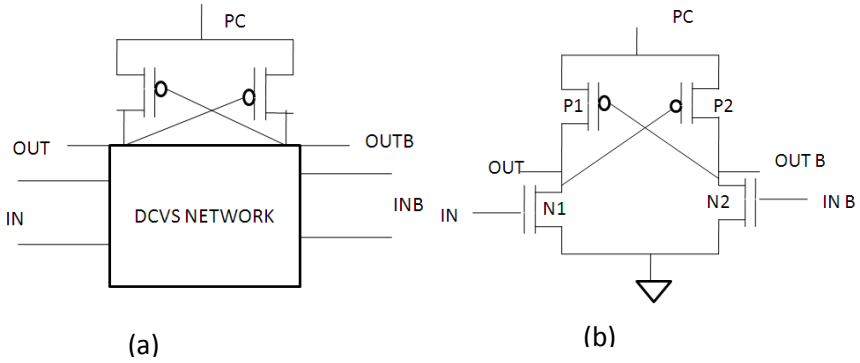

Fig.2 (a) ECRL LOGIC block diagram (b) Inverter/Buffer circuit

ECRL requires DCVS (differential cascaded voltage switching) network applying differential input then getting differential output. Fig2 (b) shows Implementation of Inverter from using ECRL block diagram shown in fig 2(a).So there is no need of extra inverter circuit to implement buffer so both inverter/buffer circuits implemented using DCVS network. ECRL requires sinusoidal power supply (PC) shown in fig3.

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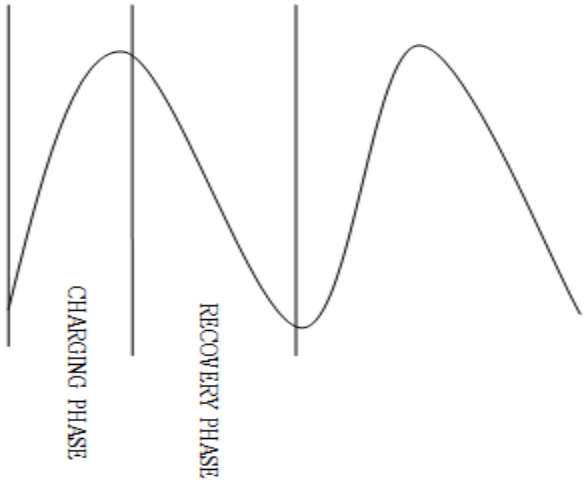

Fig.3 Sinusoidal Power supply

During the charging phase energy transfer to the load capacitance gets charged to the required voltage and during recovery phase energy stored in the capacitor is restored as supply as shown in fig3.

The operation of the ECRL inverter/buffer can be summarized using fig2 (b). Assuming the complementary outputs (out and out) are initially low and power supply ramps from logic 0 to logic 1 (v=1. 8). Now if input IN=1 and INB=0 then transistor N1 turns ON and transistor N2 turns OFF then OUT =0 and transistor P2 will be turned on then OUTB node gets charged to the logic 1 by following sinusoidal power supply charging phase. During recovery phase OUTB node is discharged through the same path in the charging path, then resultant full swing can be obtained in OUTB node. Output voltage swing for an adiabatic inverter at 100MHz frequency with a load capacitance of 10fF is shown in fig 4.

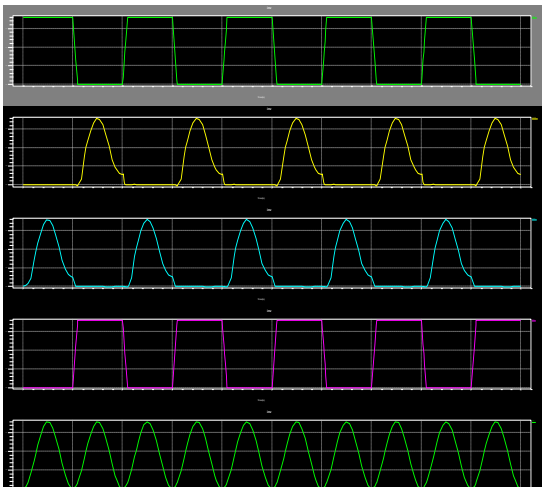

Fig.4 simulation results of ECRL inverter at 100MHz frequency with a load capacitance of a10fF

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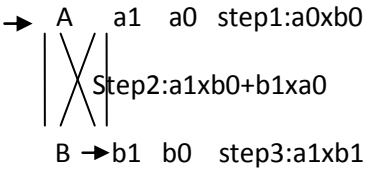
IV. IMPLEMENTATION OF NXN VEDIC MULTIPLIER

Urdhva-Tiryak bhyam sutra

The proposed multiplier is based on an algorithm Urdhava Tiryakbham (vertical and crosswise), A general multiplication formula of ancient Vedic mathematics, The parallelism in generation of partial products and their summation is obtained using urdhava tiryakbham sutra.

2x2 Vedic Multiplication algorithms:



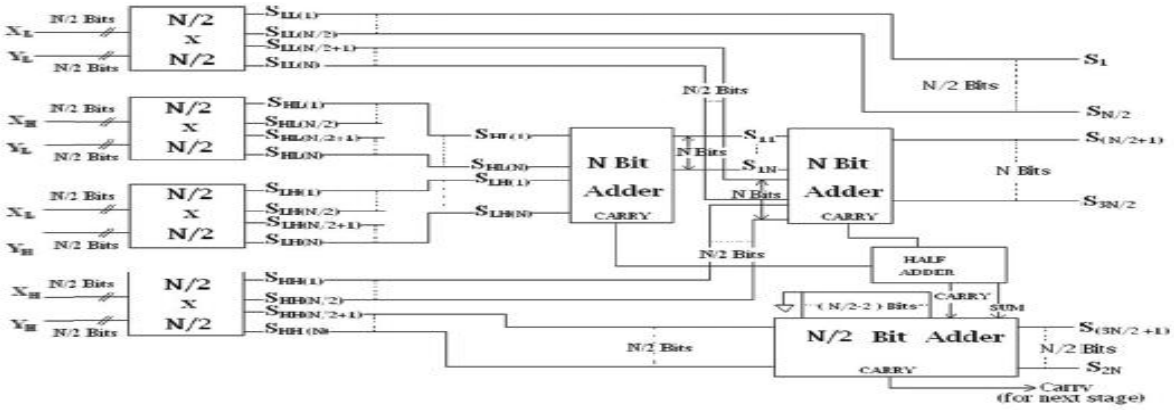


Fig.5 Block diagram of NxN Vedic multiplier

The general block diagram of NxN Vedic multiplier is shown in fig 5.So to implement NxN multiplier we require four $\frac{N}{2} x \frac{N}{2}$ Multipliers and two N bit adders, a half adder and $\frac{N}{2}$ Bit adder.

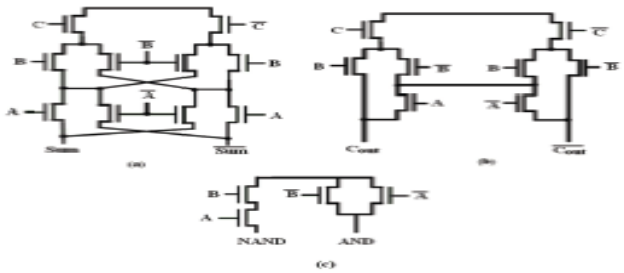


Fig.6 DCVS network (a) Sum block (b) Carry block (c) And/NAND gate

10.15662/ijareeie.2014.0308018

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We have designed a standard cell library for individual gate such as sum block, carry block, AND gate by replacing DCVS network in ECRL logic shown in fig 2 with corresponding sum block, carry block, AND gate shown fig 6. Make use of these cells, we have designed FULL adder, half adder, and a multiplier block of variable bit length using tanner tool.

V.EXPERIMENTAL RESULTS AND COMPARISON

During simulation, we have been applied 1.8V supply voltage, A= [a7, a6, a5, a4, a3, a2, a1, a0] and B= [b7, b6, b5, b4, b3, b2, b1, b0] as inputs. The pattern of inputs applied is all ones and simulation results are shown in fig 7.

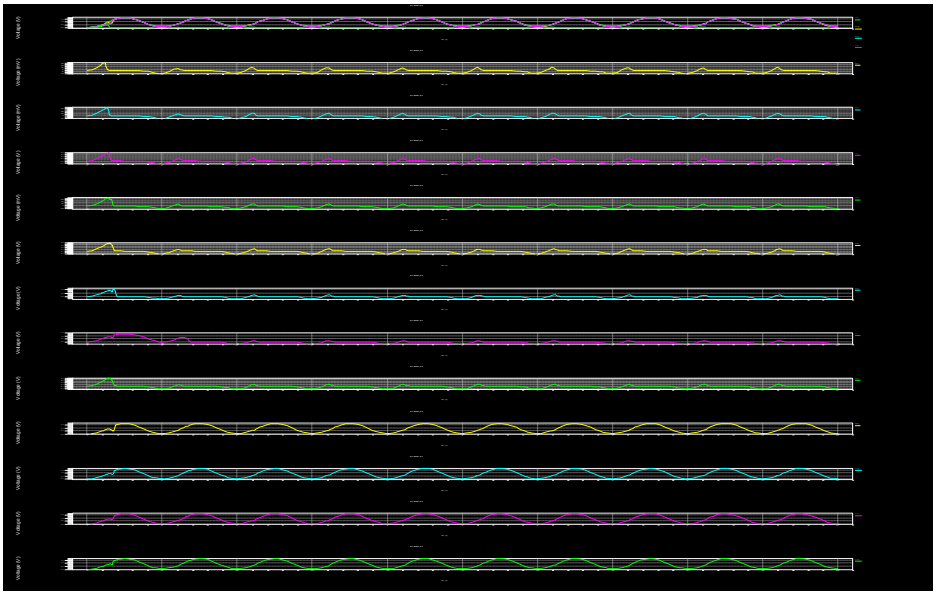

Fig.7 Simulation results of 8x8 Vedic multiplier using ECRL logic

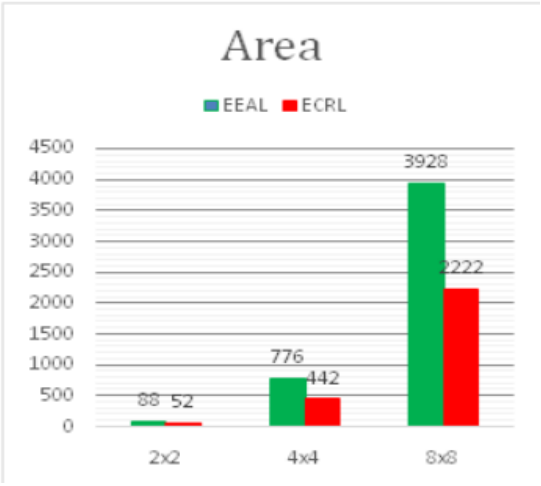

Fig.8 Comparison of the number transistors utilized

10.15662/ijareeie.2014.0308018

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Fig.9 comparison of power consumption(µW)

In Fig 8,The number of transistors utilization for 2x2, 4x4 and 8x8 is reduced by 40.9%, 43.04%and 43.43%, respectively .Also Power consumption reduced by 18.2%, 55.08% and 50.66% respectively for 2x2,4x4 and 8x8 Vedic multiplier . Power consumption of both EEAL and ECRL logic shown in fig 9.

VI. CONCLUSION

A low power area efficient adiabatic structure based on the urdhava triyakbham sutra of Vedic mathematics has been proposed using ECRL logic. It can be concluded that utilization of the number of transistors has been reduced compared to the EEAL logic. Also concluded that power Consumption can be enhanced in the proposed adiabatic logic.

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