ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 8, August 2014

A Greedy Heuristic Algorithm for Flip-Flop Replacement Power Reduction in Digital Integrated Circuits

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ABSTRACT: Power consumed by clocking has taken a major part of the whole design circuit. This paper proposed that reducing the power consumption and area by replacing some flip flops with fewer multi-bit flip-flops without affecting the performance of the original circuit. Various techniques are proposed. First to identify those flip-flops that can be merged. Next a combination table is built to enumerate all possible combinations. Finally, those flip-flops are merged in hierarchical manner. Besides the power reduction minimizing the total wire length is also considered. According to the experimental results clock power can be reduced by 20-30% and the running time can also be reduced

KEYWORDS: Clock power reduction, merging, wire length, replacement, multi-bit flip-flop.

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I.INTRODUCTION

A clock system and a logic part consumes dominant Part of the total chip power by 20–45%. In this clock system power, 90% is consumed by the flip-flops [1]. This is due to the high switching activity.

$$P_{clk} = C_{clk} V^2_{dd} f_{clk} \qquad (1)$$

Where *Pclk is* clock power, *fclk* is the clock frequency, *Vdd* is the supply voltage, and *Cclk* is the switching capacitance included in the gate capacitance of flip-flops.

During clock tree synthesis, less number of flip-flops means less number of clock sinks. Thus the resulting clock network would have smaller power consumption and uses less routing resource. The total power is reduced by replacing the 2 bit flip-flops with two 1-bit flip-flops since the two flip flops consume the same clock. However the locations of some flip-flops would be changed after this replacement and thus the wire-lengths of nets connecting pins to a flip- flop are also changed.

Single-bit flip-flop can be reviewed before using the multi bit flip-flop. Figure 1.1 shows an example of single-bit flip-flop. A single-bit flip-flop has two latches (Master latch and slave latch).The latches need “Clk” and “Clk’ ” signal to perform operations, shown in Figure1.

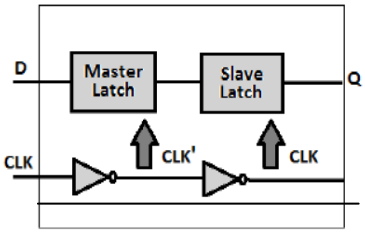

Fig. 1: Single-Bit Flip-Flop

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 3, Issue 8, August 2014

In order to have better delay from Clk-> Q, regenerate "Clk" from "Clk'". There are two inverters in the clock path. Figure 2 shows an example of merging two 1-bit flip-flops into one 2-bit flip-flop. Each 1-bit flip-flop contains two inverters, master-latch and slave-latch. Due to the manufacturing rules, inverters in flip-flops tend to be oversized.

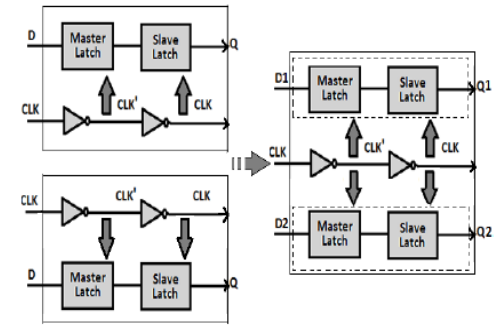

Fig. 2: Merging flip-flops

As the process technology advances into smaller geometry nodes, the minimum size of clock drivers can drive more than one flip-flop. Merging single-bit flip-flops into one multi-bit flip-flop can avoid duplication inverters and lowers the total clock dynamic power consumption.

II. LITERATURE SURVEY

1) P. Gronowski, W. J. Bowhill, R. P. Preston, M. K. Gowan, and R.L.Allmon, "Post placement power optimization with Multi Bit Flip- Flop," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 676–686, May 2012.

Concept:

Replacing several one bit flip flop with one Multi Bit Flip Flop to reduce the total area and dynamic power and it can be reduced upto 50%.

Disadvantage:

Windows optimization technique is larger so that flip flop can perform slowly .

2) D. Duarte, V. Narayanan, and M. J. Irwin, "Power aware placement," in *Proc. IEEE VLSI Comput. Soc. Annu. Symp.*,Pittsburgh, PA, Apr. 2005, pp. 52–57.

Concept:

Focuses on calculating the idle period of different flip flop and inserting the gating logic into netlist to achieve the total power by 25.3%.

Disadvantages:

The net switching power can be achieved by 25.4 % and then wirelength can also be reduced.

3) H. Kawagachi and T. Sakurai, "Impact of technology scaling in the clock power," in *VLSI Circuits Dig. Tech. Papers Symp.*, Jun. 2003, pp. 97–98.

Concept:

Increase the flexibility that covers the clock distribution and clock generation circuit to consume total power by 40%.

Disadvantage:

Clock skew problem can be reduced by 30%.

4)W. Hou, D. Liu, and P.-H. Ho, "Automatic register banking for low power clock trees," in *Proc. Quality Electron. Design*, San Jose, Mar. 2010, pp. 647–652

Concept:

Replacing some flip flop with multibit flip flop without affecting the performance and total wire length can be minimized by 20-30%.

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Disadvantage:

Using dual bit flip flop to save the clock power in 11 .22% and the replacement of flip flop during switching rate is 10.43%.

5) Y. Cheon, P.-H. Ho, A. B. Kahng, S. Reda, and Q. Wang, "High performance microprocessor design," in *Proc. Design Autom. Conf.*, Jun. `1998, pp. 795–800.

Concept:

Focuss on high frequency design to achieve high performance and to improve the complexity of the circuit.

Disadvantage:

In single supply voltage system reduce the clock power 25.45 %, and in multiple supply voltage system the clock power can be reduced by 26.15 %.

III.PROPOSED ALGORITHM

The Design flow can be roughly divided into three stages. First to use the combination table to combine all possible combinations of flip-flops. The difficulty of this problem is to repeatedly search a set of flip-flops that can be replaced by a new multi-bit flip-flop. However as the number of flip-flops in a chip increases dramatically the complexity would increase exponentially which makes the method impractical. To handle this problem more efficiently and to get better results, the following flowchart were used. The figure 3 shows the various approaches used in the algorithm.

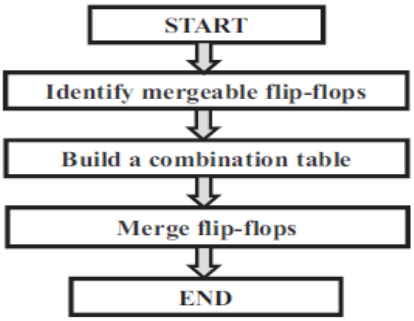

Fig. 3: Flow chart of proposed method

1) To facilitate the identification of mergeable flip- flops transform the coordinate system of cells. In this way the memory used to record the feasible placement region can also be reduced.

2) To avoid wasting time in finding impossible combinations of flip-flops, first build a combination table before actually merging two flip-flops. For example, if a library only provides three kinds of flip-flops which are 1-, 2-, and 3-bit first to separate the flip-flops into three groups. Therefore the combination of 1- and 3-bit flip-flops is not considered since the library does not provide the type of 4-bit flip-flop.

3) Partition a chip into several sub regions and perform replacement in each sub region to reduce the complexity. However, this method may degrade the solutions quality. To resolve the problem use a hierarchical way to enhance the result

A. Region partition to identify the mergeable flip-flop

To reduce the complexity, first divide the whole placement region into several sub-regions and then by using the combination table replace the flip-flops in each other sub- region. Then several sub-regions are combined into a larger sub-region and the flip-flops are replaced again so that those flip-flops in the neighboring sub-regions can be replaced further. Finally those flip-flops with pseudo types are deleted in the last stage as it is not provided by the supported library.

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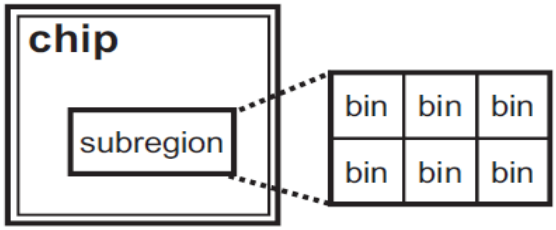

Fig. 4: Region partition with six bins in one sub-region

B. Replacement of flip-flop

After a combination has been built do the replacements of flip-flops according to the combination table. First flip-flops below the combinations corresponding to their types in the library were linked. Then for each combination **n** in **T,** serially merge the flip-flops linked below the left child and the right child of **n** from leaves to root. Based on its binary tree to find the combinations associated with the left child and right child of the root. Hence the flip-flops in the lists named left and lright, linked below the combinations of its left child and its right child are checked. Then for each flip-flop **f i** in lleft the best flip-flop fbest in lright which is the flip-flop that can be merged with **f i** with the smallest cost recorded in cbest, is picked. For each pair of flip-flops the combination cost is computed and they can be merged with the smallest cost as chosen. Finally add a new flip-flop **f** in the list of the combination n and remove the picked flip-flops which constitutes the **f** .For example, given a library containing three types of flip-flops (1-, 2-, and 4-bit), first to build a combination table **T** as shown in Figure5.

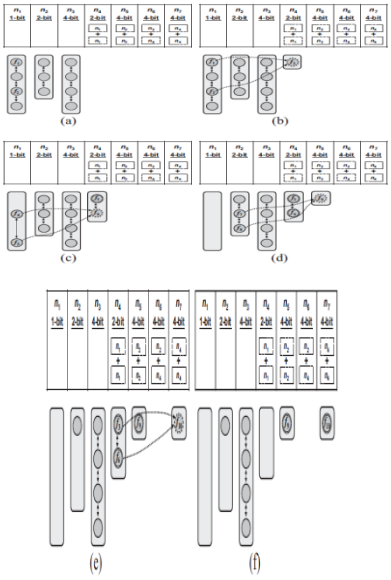

Fig. 5: Replacements of flip-flops.

The above figure says that
(a) Sets of flip-flops before merging.
(b) Two 1-bit flip-flops, f1 and f2, are replaced by the 2-bit flip-flop f3.
(c) Two 1-bit flip-flops, f4 and f5, are replaced by the 2-bit flip-flop f6.
(d) Two 2-bit flip-flops, f7 and f8, are replaced by the 4-bit flip-flop f9.
(e) Two 2-bit flip-flops, f3 and f6, are replaced by the 4-bit flip-flop f10.
(f) Sets of flip-flops after merging.

In the beginning, the flip-flops with various types are, respectively, linked below *n*1, *n*2, and *n*3 in ***T*** according to their types. Suppose to form a flip-flop in *n*4 which needs two 1-bit flip-flops according to the

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ISSN (Online): 2278 – 8875

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combination table then each pair of flip-flops in *n*1 are selected and checked to see if they can be combined .If there are several possible choices the pair with the smallest cost value is chosen to break the tie.

C. Combination table and merging flip-flop

Finally add a new flip-flop **f** in the list of the combination n and remove the picked flip-flops which constitutes the **f** .Pseudo type is an intermediate type which is used to enumerate all possible combinations in the combination table **T**, then to remove the flip-flops belonging to pseudo types. Thus after the above procedures have been applied de-replacement and replacement functions are performed if there exists any flop-flops belonging to a pseudo type is shown in figure 6

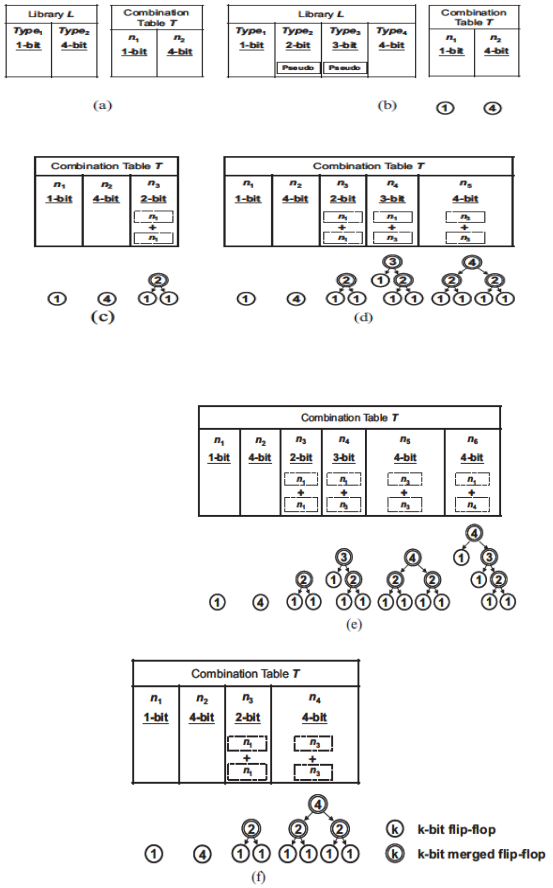

Fig. 6 : The combination table and merging

The figure says that

(a) Initialize the library *L*and the combination table *T* .

(b) Pseudo types are added into *L*, and the corresponding binary tree is also build.

(c) New combination *n*3 is obtained from combining two *n*1s. (d) New combination *n*4 is obtained from combining *n*1 and *n*3.

(e) New combination *n*6 is obtained from combining*n*1 and *n*4. (f) Last combination table is obtained after deleting unused combination in (e).

For example, if there still exists a flip-flop, fi , belonging to n3 after replacements in Fig (Fig. Last combination table is obtained after deleting the unused combination), then to de-replace fi into two flip-flops originally belongs to n1. After de-replacing, the replacements of flip-flops according to **T** without consideration of the combinations whose corresponding type is pseudo in **L** were built

10.15662/ijareeie.2014.0308076

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IV. COMPARISON TABLE FOR VARIOUS METHODS

This table specifies the various implementation of flip-flop to optimize the power and to achieve the net switching activity. Although the drivers are very wide devices it was found that for all technologies the share of the clock power that is due to leakage is at most 2.5%. Technology optimizations and dynamic runtime techniques forleakage reduction will become standard for clock power and will remain a major contributor to the total system power.

Implementation	Description	Motivation
Post Placement Power Optimization	Progressive Windows Based Optimization	Reduce The Power & Interconnecting Wire length
Power Aware Placement.	Register clustering & net weighting	Reduced area &wire length
Impact Of Technology Scaling	Scaling interconnect & impact of leakage	Reduced leakage power
Flip-Flop Merging And Relocation	Net Switching technique	Switching rate less &save clock power
Clock Power Using Multibit Flip-flop	Three phase algorithm	Reduced power single & multiple supply voltage system
Clock Power Flip-Flop For Future Soc Applications	CDMFF + CPSFF Proposed in LCPTFF	Reduced power &area
A Low-Swing Clock Double-Edge Triggered Flip-Flop	LCDFF performed charging &discharging Technique	Saving power in flip-flop operation & clock network

CONVENTIONAL CONDITIONAL DATA MAPPING
D FLIP-FLOP

In conditional data mapping flip-flop (CDMFF) uses only seven clocked transistors, resulting in about 50% reductions in the number of clocked transistors. This shows the effectiveness of reducing clocked transistor numbers to achieve low power. The figure 7 shows the circuit diagram for CDMFF

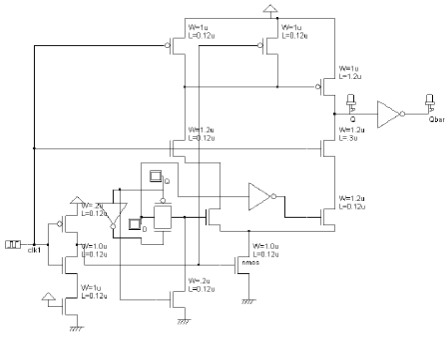

Fig. 7: Circuit diagram of CDMFF

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In a Conventional D flip-flop part of the clock energy is consumed by the internal clock buffer to control the transmission gates.

CLOCKED PAIR SHARED FLIP-FLOP DESIGN

To ensure efficient and robust implementation of low power sequential element propose a Clocked Pair Shared flip-flop to use less clocked transistor than CDMFF and to overcome the floating problem in CDMFF.The figure 8 shows the block diagram of CPSFF

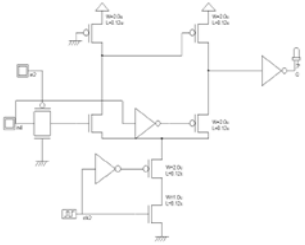

Fig. 8: Circuit diagram of CPSFF

By reducing the no of transistor count the overall switching delay, power, and area consumption can be reduced. LOW POWER CLOCKED PASS TRANSISTOR FLIP- FLOP Low Power Clocked Pass Transistor flip-flop design shows much less power & Area constraints than the Existing two Flip-Flop designs. LCPTFF will be having very less clock delay when compared to all other circuits.

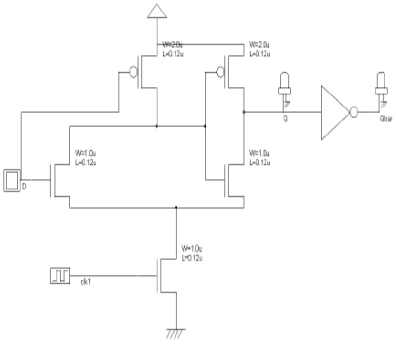

Fig. 9: Circuit diagram of LCPTFF

Type	Power Consumption	Area Consumption
Conventional CDMFF Design	0.45mW	270µm^2
Clock Pair Share Flip-Flop (CPSFF)	15.232µW	225 µm^2
Proposed Design (LCPTFF)	9.581 µW	84 µm^2

Table 1: Comparison table for Power and Area

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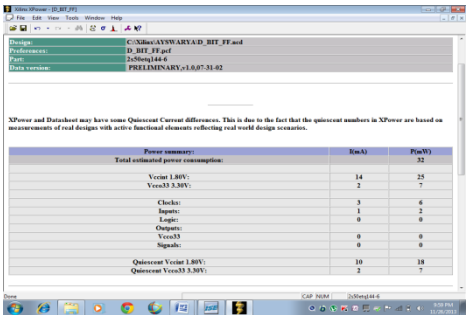
IV.SIMULATION RESULTS



FOR D BIT FLIP-FLOP

```
Xilinx Mapping Report File for Design 'D_BIT_FF'

Design Information
------------------
Command Line   : C:\Xilinx\bin\nt\map.exe -ise
E:/    AISWARYA /PROJECTS/PROCESSED/CHV0189--MULTIBIT_FF/TEST/TEST.ise -intstyle
ise -p xc2s100e-tq144-7 -cm area -pr b -k 4 -c 100 -tx off -o D_BIT_FF_map.ncd
D_BIT_FF.ngd D_BIT_FF.pcf
Target Device  : xc2s100e
Target Package : tq144
Target Speed   : -7
Mapper Version : spartan2e -- $Revision: 1.34 $
Mapped Date    : Fri Oct 19 09:59:19 2012

Design Summary
--------------
Number of errors:     0
Number of warnings:   0
Logic Utilization:
Logic Distribution:
   Number of Slices containing only related logic:     0 out of     0   0%
   Number of Slices containing unrelated logic:        0 out of     0   0%
      *See NOTES below for an explanation of the effects of unrelated logic
   Number of bonded IOBs:           4 out of    98   4%
      IOB Flip Flops:                          4
   Number of GCLKs:                 1 out of     4  25%
   Number of GCLKIOBs:              1 out of     4  25%

Total equivalent gate count for design:  32
```

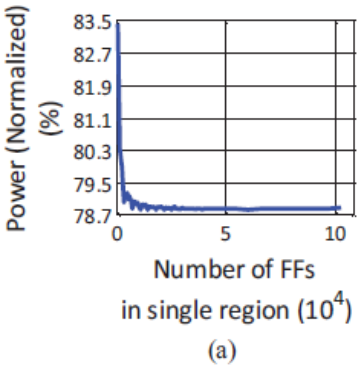


Fig:10 a) Influence of the region size on power

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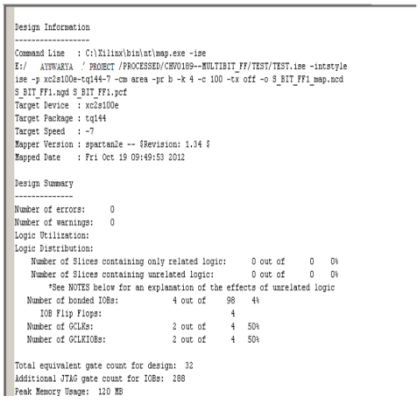
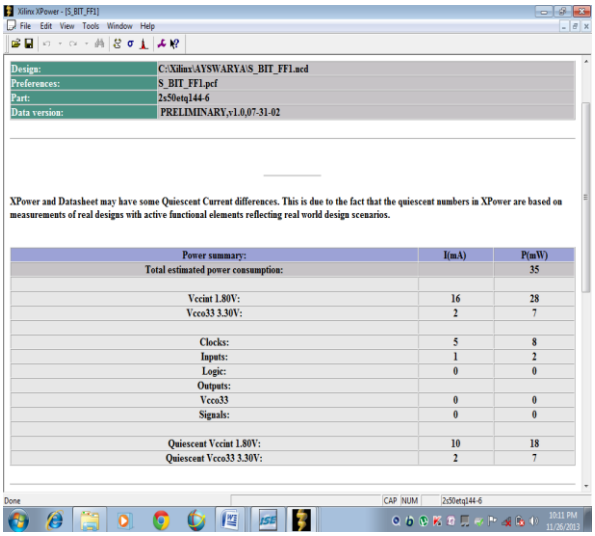
FOR S BIT FLIP-FLOP



```
Design Information
------------------
Command Line   : C:\Xilinx\bin\nt\map.exe -ise
E:/   AYSWARYA   / PROJECT /PROCESSED/CHVU189--MULTIBIT_FF/TEST/TEST.ise -intstyle
ise -p xc2s100e-tq144-7 -cm area -pr b -k 4 -c 100 -tx off -o S_BIT_FF1_map.ncd
S_BIT_FF1.ngd S_BIT_FF1.pcf
Target Device  : xc2s100e
Target Package : tq144
Target Speed   : -7
Mapper Version : spartan2e -- $Revision: 1.34 $
Mapped Date    : Fri Oct 19 09:49:53 2012

Design Summary
--------------
Number of errors:     0
Number of warnings:   0
Logic Utilization:
Logic Distribution:
   Number of Slices containing only related logic:      0 out of      0   0%
   Number of Slices containing unrelated logic:         0 out of      0   0%
      *See NOTES below for an explanation of the effects of unrelated logic
   Number of bonded IOBs:             4 out of     98   4%
      IOB Flip Flops:                 4
   Number of GCLKs:                   2 out of      4   50%
   Number of GCLKIOBs:                2 out of      4   50%

Total equivalent gate count for design:  32
Additional JTAG gate count for IOBs:  288
Peak Memory Usage:  120 MB
```



Xilinx XPower - [S_BIT_FF1]

File Edit View Tools Window Help

Design:	C:\Xilinx\AYSWARYA\S_BIT_FF1.ncd
Preferences:	S_BIT_FF1.pcf
Part:	2s50etq144-6
Data version:	PRELIMINARY,v1.0,07-31-02

XPower and Datasheet may have some Quiescent Current differences. This is due to the fact that the quiescent numbers in XPower are based on measurements of real designs with active functional elements reflecting real world design scenarios.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		35
Vccint 1.80V:	16	28
Vcco33 3.30V:	2	7
Clocks:	5	8
Inputs:	1	2
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	10	18
Quiescent Vcco33 3.30V:	2	7

Done CAP NUM 2s50etq144-6

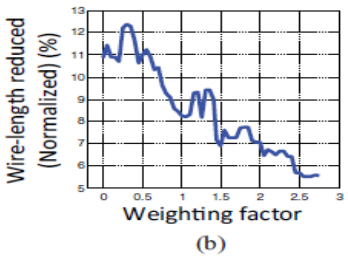


Fig:11 b) Influence of the weighting factor on Wire-length reduction

OUTPUT WAVEFORM

The values PR_Ratio and WR_Ratio can be computed by the following equations:

$$PR_{Ratio\ (\%)} = \frac{Power_{original} - Power_{merged}}{Power_{original}} \times 100\%$$

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$$W_{R_{Ratio\,(\%)}} = \frac{wire\_length_{merged}}{wire\_length_{original}} \times 100\%$$

Table 2: Comparison of simulated results

Parameters	Existing Flip-Flop	Merged Flip-Flop
Power	32	35
Wire length	35	42

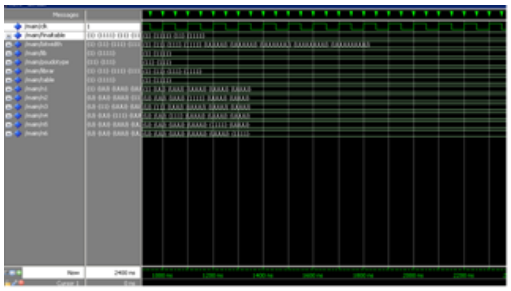

Fig:12 Simulation result of combinational Table

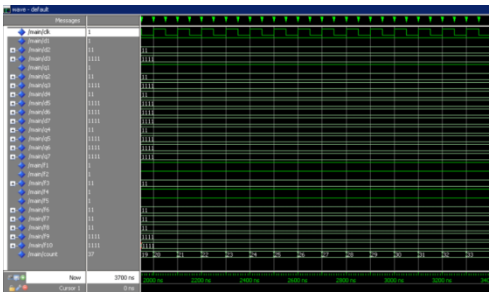

Fig:13 Simulation results of merged flipflop

V.CONCLUSION

The number of flip-flops in a chip increases dramatically the complexity would increase exponentially, which makes the method impractical. To handle this problem more efficiently and get better results, the following approaches are used.1) To facilitate the identification of mergeable flip-flops transform the coordinate system of cells. In this way the memory used to record the feasible placement region can also be reduced.2) To avoid wasting time in finding impossible combinations of flip-flops first build a combination table before actually merging two lip-flops.3) Partition a chip into several sub-regions and perform replacement in each sub-region to reduce the complexity. However this method may degrade the solution quality. To resolve the problem use a hierarchical way to enhance the result and processing time can be reduced.

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