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A New Self-Balancing Cascaded Multilevel Inverter for Level Doubling Application

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ABSTRACT: A novel level doubling network (LDN) based multilevel inverter (MLI) topology is proposed in this paper. The LDN takes only two switches, which is formed by half-bridge inverter to almost double the number of output voltage levels. The concept (of the proposed LDN) has the capability of self-balancing during positive and negative cycles without any closed-loop control/algorithm. The topology has uses a symmetric cascaded H-bridge MLI. The proposed self-balanced multilevel inverter has eliminates the harmonics level and reduces the number number of switches and losses; which has provide better results compares with conventional six bridge multilevel inverter. The simulation results are verified in MATLAB/SIMULINK model.

KEYWORDS: Cascaded multilevel inverter developed H-bridge, multilevel inverter, level doubling network (LDN), self-balanced multilevel inverter (MLI), power quality.

I.INTRODUCTION

Multilevel inverters offer various applications in voltage ranging from medium to high such as in renewable energy sources, industrial, laminators, blowers, fans, and conveyors. Small voltage step results in making the multilevel inverters withstand better voltage, lower harmonics, good electromagnetic compatibility, minimized switching loss, and better power quality[1][2]. Cascaded multilevel inverters were developed in the initial stage. Later, diode- lamped MLI'S were developed followed by lying capacitor MLI'S. These three topologies utilize different mechanisms to produce the required output. the topology introduced first, that is, the CMLI, is simply series connection of H-bridges[4][5].

The cascaded multilevel inverter has more advantages than other two topologies [6], [7], since it does not require any balancing capacitors and diodes. Cascaded inverter needs separate DC sources for each H-Bridge, hence there is no voltage balancing problem, but isolated DC sources are not readily available, this could be main drawback of this topology[3]. Cascaded topology requires more switches.

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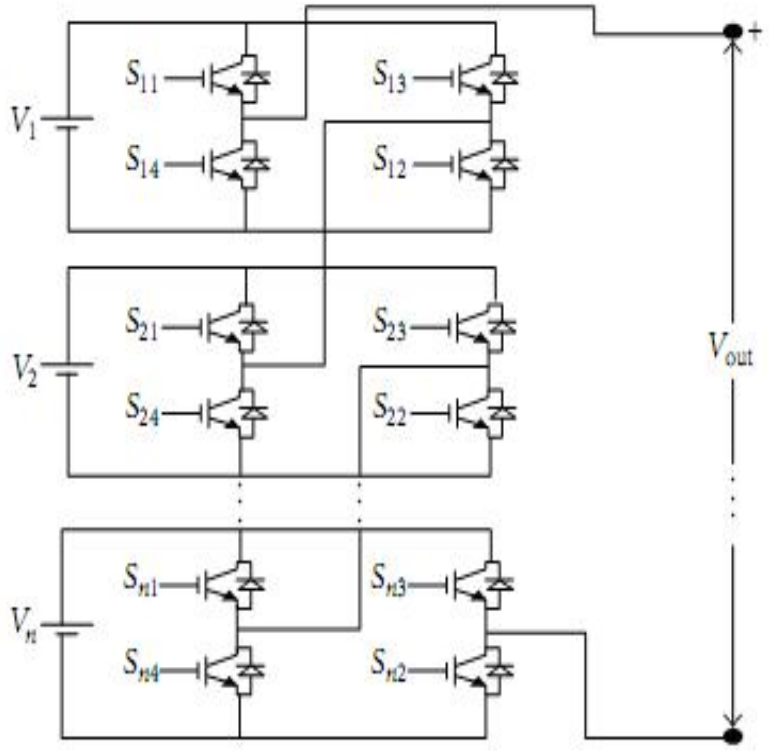

Fig. 1 Conventional cascaded n-level MLI.

Conventional Topology**.** Using 3 DC voltage sources, 3 H-bridge units each with 4 switches together forming 12 switches in total are used in conventional CMLI which is represented in Figure 1.General expression for output voltage levels, M = (n + 2)/2 where n is the number of switches in the configuration. Each Bridge is outputting 3 Levels, +Vdc, 0, −Vdc. Cascading 3 Bridges in such a fashion to produce stepped 7 level staircase waveforms.

Cascaded H-bridge (CHB) MLI is obtained high-quality output voltages and input currents, high reliability due to their intrinsic component redundancy [8] [10]. One of the main technique is induced to increase the number of levels is by asymmetry in voltage ratio of the inverter cells. The asymmetric structure of the MLI is introduced in [4] and [5] and is capable to produce a very high number of levels with a given switch count [2]. For a given topology, the number of levels depends on the configuration of the dc voltage ratio(leading to binary, trinary, and other configurations). in asymmetric structure, powers delivered by the various levels are quite different [8]. While most of the power is delivered by the highest voltage cell [6], the lower voltage cells deal with only a fraction of the same.

A floating scheme is presented in binary MLI [7]. This topology proposes, special attention of voltage balancing problem demanding complex control algorithms. This is suitable for high-power applications. Higher voltage and higher number of levels are achieved using low-voltage switch-based power converters and summing transformer. In this topology, high-voltage switches are avoided at the cost of summing transformers. Neutral point clamped (NPC)-CHB hybrid and asymmetric topology are introduced in [9]. A CHB with a dc bus voltage lower than NPC is connected in between the NPC terminal and the load terminals to obtain finer and more numbers of voltage steps. This topology also requires special attention to take care of the voltage balancing problem. This paper proposes a new topology to almost double the number of levels in an MLI, by adding only two switches per phase.

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II.PROPOSED TOPOLOGY

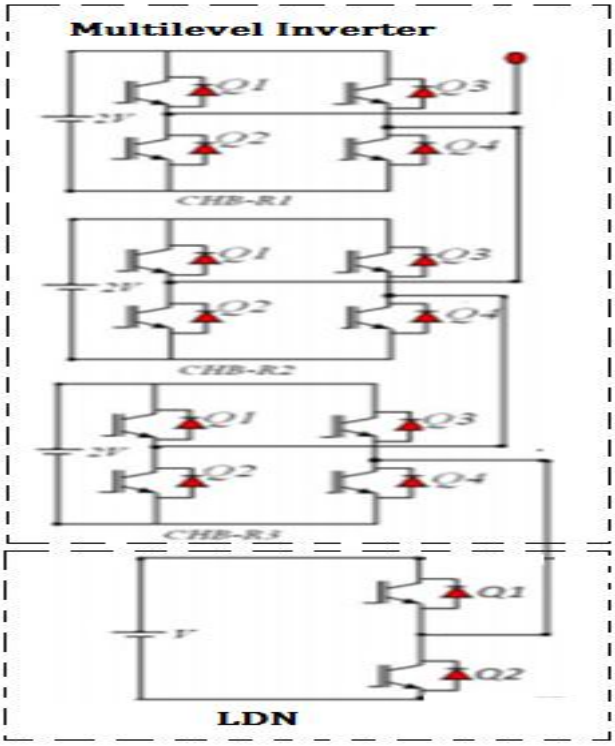

Fig. 2. Circuit diagram of the proposed topology (single-phase version).

This does not allow the bridges to be easily replaced (as the high side and low side bridges most likely to be made by different power devices) and hence loses the advantage of modularity. This makes the asymmetric topology not very attractive for medium-voltage (MV) drives and many other applications. Recently, many hybrid multilevel topologies are proposed [10]–[11]. However, the symmetric CHB structure has definite merits in high-power applications due to fault tolerance/reliability and modularity. The recent trend is to use a symmetric MLI fed by a multipulse rectifier [12]–[13] for high- and medium-power applications in industry. Balance its floating capacitor. The capacitors here maintain the voltage by virtue of the self-balancing property of the topology, detailed at a later stage in this work.

The single-phase version of the proposed topology is shown in Fig. 1. The topology is realized by adding an extra half-bridge connected to a capacitor that maintains half the voltage of other bridges by a self-balancing mechanism. For a three-phase system, three half-bridges (i.e., one half-bridge per phase) in parallel are required. Thus, effectively, a three-phase full-bridge needs to be connected as shown in Fig. 2. Note that the dc buses of these half-bridges do not consume any power. If this delivers a given amount of power in the first half cycle, it will absorb the same amount of power in the next half cycle.

From this study of operation, we get N additional levels in the positive half cycle with the output voltage: V/2, 3V/2, 5V/2,., (2N − 1)V/2 (by adding voltage V/2 with 0, V , 2V,..., (N − 1)V , respectively, in the positive half cycle). Similarly, on the other half cycle, N additional levels are obtained (i.e., −V/2, −3V/2, −5V/2,...,−(2N − 1)V/2). However, the difference with the first half cycle is that the levels are obtained by algebraically summing the half-bridge voltage V/2 with −V,−2V,−4V,−NV,respectively. Therefore, in the second half cycle, the dc bus of the half-bridge will be equally charged. Finally, at the end of one complete cycle, the dc bus voltage of the half-bridge will ideally remain unchanged. This will remain valid for any power factor (as the power distribution ratio of MLI is independent of power factor.

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TABLE1: SWITCHING TABLE

	BRIDGE1 (2V)				BRIDGE2 (2V)				BRIDGE 3 (2V)				HB (V)	
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2
-6V	0	1	1	0	0	1	1	0	0	1	1	0	0	1
-5V	0	1	1	0	0	1	1	0	0	1	1	0	1	0
-4V	0	1	1	0	0	1	1	0	0	1	0	1	0	1
-3V	0	1	1	0	0	1	1	0	0	1	0	1	1	0
-2V	0	1	0	1	0	1	0	1	0	1	1	0	0	1
-1V	0	1	0	1	0	1	0	1	0	1	1	0	1	0
0V	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1V	0	1	0	1	0	1	0	1	0	1	0	1	1	0
2V	0	1	0	1	0	1	0	1	1	0	0	1	0	1
3V	0	1	0	1	0	1	0	1	1	0	0	1	1	0
4V	1	0	0	1	1	0	0	1	0	1	0	1	0	1
5V	1	0	0	1	1	0	0	1	0	1	0	1	1	0
6V	1	0	0	1	1	0	0	1	1	0	0	1	0	1

A switching table is thus formed for the proposed inverter with three CHBs per phase (as shown in Table I). bridges1, 2, and 3 are of equal voltage. Bridge4 is at a voltage half of other cells and having only two switches (due to half-bridge configuration). For a poly phase system, these LDNs of all phases may be connected to a common dc bus and will also help in reducing the dc bus current ripple (with corresponding reduction in dc bus capacitance)[14]-[16]. It is important to note that, for N number of voltage cells, the symmetry restricts the maximum voltage.

The energy delivered/absorbed (by the LDN) at any nth interval is

$$W_{1st} = VI_m \int_{\theta_{2N-1}\neq\emptyset}^{\theta_{2N}} sin\theta d\theta \quad (1)$$

$$W_{2nd} = VI_m \sum_{n=2N+1}^{4N} \int_{\theta_{2N-1}\neq\emptyset}^{\theta_{2N}} sin\theta d\theta \quad (2)$$

$$W_{1st} = -W_{2sd} \quad (3)$$

Hence, the energy delivered/absorbed in first half cycle will be equal to the energy absorbed/delivered by LDN in the next half cycle.

III.CONTROL STRATEGIES

PWM technique will cause extra losses due to high switching frequencies. For this reason, low-switching frequency control methods, such as selective harmonic elimination method, fundamental frequency switching method or active harmonic elimination method, can be used for the MLI control.

It is desired that the ac output voltage VO = Van follow a given waveform (e.g., sinusoidal) on a continuous basis by properly switching the power valves. The carrier based PWM technique fulfils such a requirement as it defines the on and off states of the switches of one leg of a VSI by comparing a modulating signal VA (desired ac output voltage) and a triangular waveform VC (carrier signal).

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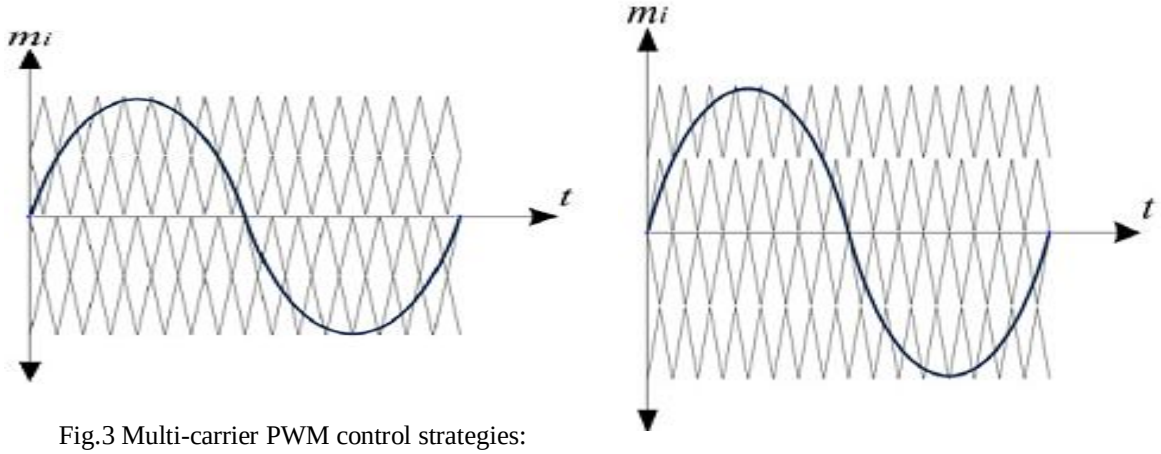

Fig.3 Multi-carrier PWM control strategies:
(a) POD (b) APOD

IV.SIMULATION RESULTS

The performance of the topology is evaluated by simulating the circuit in MATLAB/Simulink. A Simulink model is developed for the single-phase version of the proposed topology. In this section to verify multilevel output for conventional and proposed system. The output voltage and current waveforms and their total harmonic distortion (THD) are analyzed. Also, the performance of the LDN and its energy consumption are investigated. Table II shows the parameters used for simulation. Fig:4&5 shows the conventional and proposed circuit diagram. The 13level output voltage is given in fig: 6(a), (b). The THD Verification for both system are given in fig:7(a),(b).

TABLE:2 SIMULATION PARAMETER

Simulation parameter	value
Proposed scheme	
Number of H-bridges per phase	3
Inverter structure	Symmetrical
Input to DC bus of H-bridge	3
H-Bridge DC bus capacitance	100v
LDN dc bus capacitance	11,000μF
LOAD Time constant	500μs
Initial LDN voltage	0v
Conventional topology	
Number of H-bridges per phase	6
Inverter structure	Symmetrical
Input to DC bus of H-bridge	6
H-Bridge DC bus capacitance	100v
Total number of switches	24

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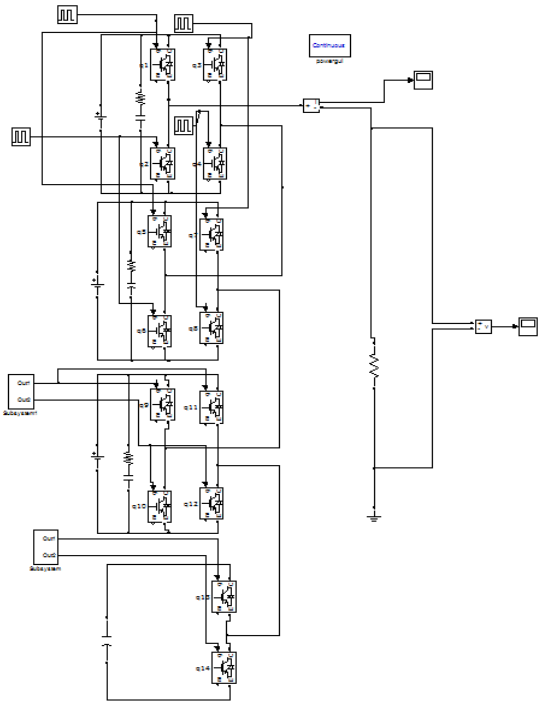

Fig.4 proposed simulation circuit

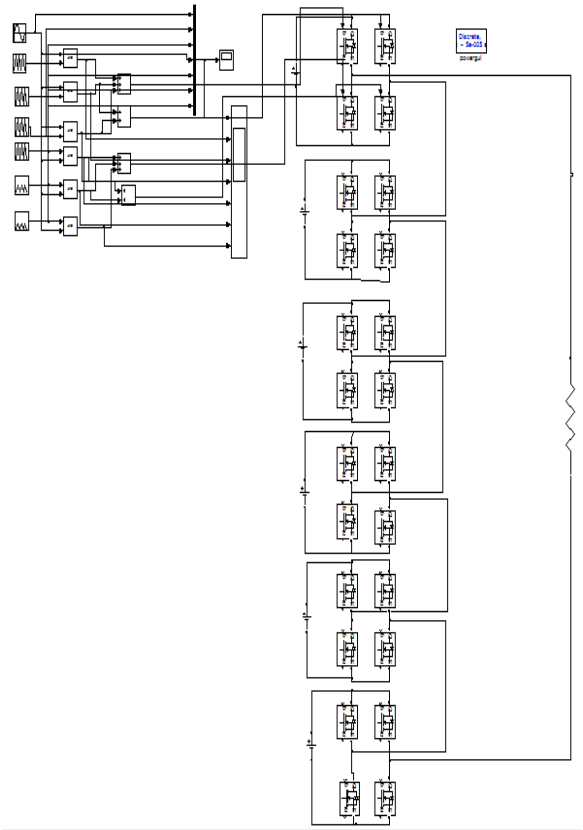

Fig.5 conventional simulation circuit

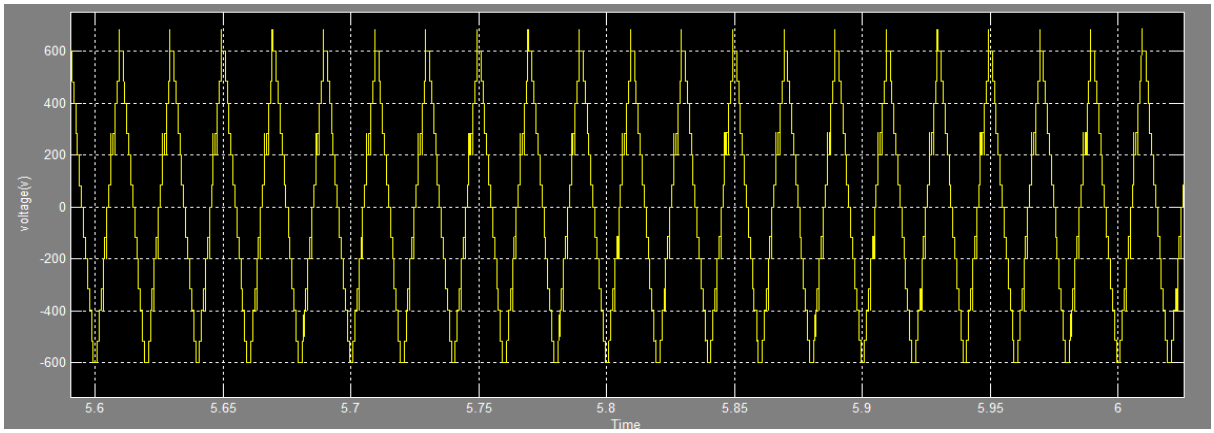

Fig.6(a) simulation results for proposed circuit : output voltage:600v

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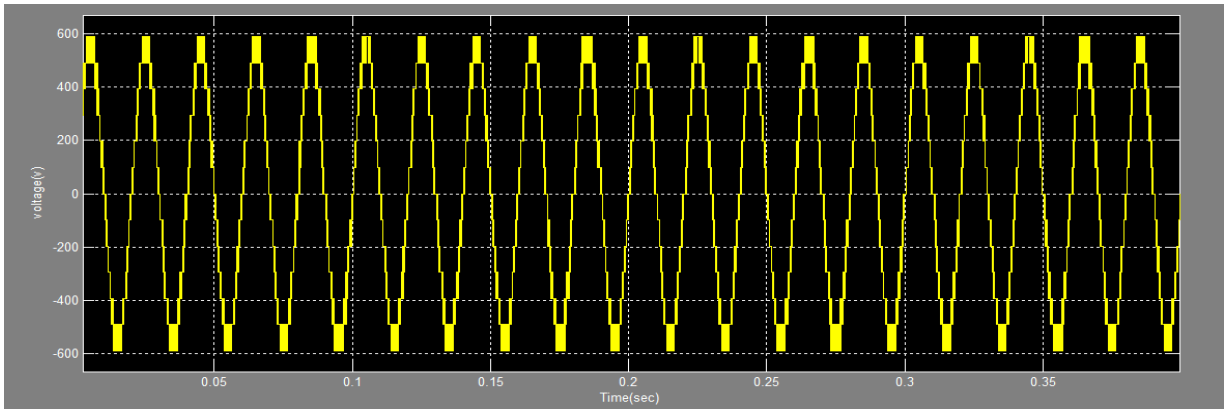

Fig. 6 (b) simulation results for conventional circuit : output voltage:600v

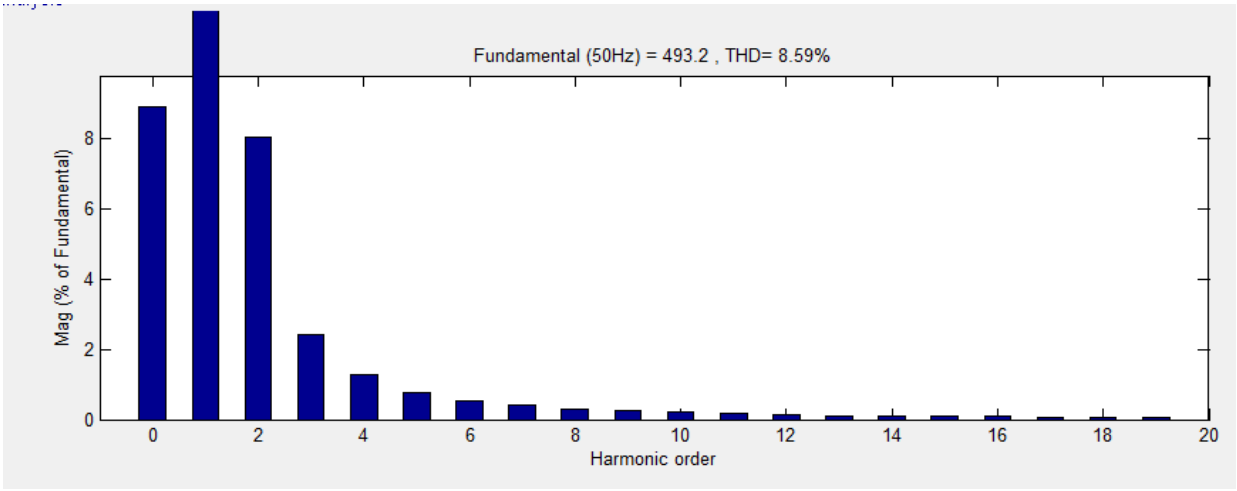

Fig.7(a) THD

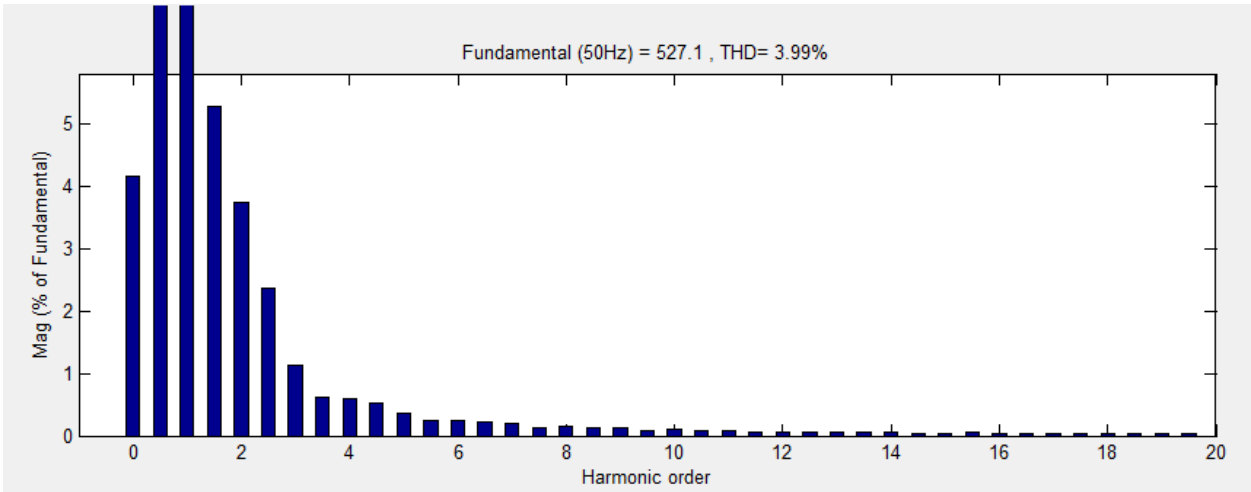

Fig. 7(b) THD

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V.CONCLUSION

This paper has presented a new concept to increase the number of levels in a cascaded MLI. A single-phase bridge network is used to almost double the number of levels of the single phase cascaded MLI. The self-balancing topology is verified. The concept may be applied for both symmetric and asymmetric topologies. The results are compared with conventional methods and the has not only increased the levels but also maintained uniform power loading of the individual cell of the cascaded configuration. The operating principle of the circuit is explained. A detailed simulation is presented using MATLAB/Simulink. The THD= 3.99 for proposed topology which is better result compared with conventional system.

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