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A Novel Methodology to Debug Leakage Power Issues in Silicon- A Mobile SoC Ramp Production Case Study

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ABSTRACT: As the world is moving toward DSM era, understanding silicon behavior is becoming more and more challenging. Models are getting complex and yet not able to reflect the actual silicon behavior. Hence some of the silicon issues cannot be replicated in circuit simulations. The problems found on silicon require the understanding of various tools and techniques available to observe and modify the die. A good understanding of these techniques and debug methodology is required to meet Time to Market goals.

The devices used for mobile applications have stringent power requirements. The devices thus have power conservation modes during which the current drawn is extremely low of the order of tens of microamperes. This paper discusses the challenges and techniques used to identify the issues found in shutdown mode (a power conservation mode), which had to be addressed in order to ramp the device to production.

KEYWORDS: Low Power, DSM, SoC, ASIC, EMMI, Mobile, Powerdown mode, Leakage Current, IDDQ, Isolation Cell, Silicon Debug

I. INTRODUCTION

In any design the total power is contributed by two components, viz. active power and leakage power. The active power consists of

- Transient power
- Cap switching power Leakage power is mainly due to
- Sub threshold leakage (Isub)
- Reverse biased diode leakage (Issat)
- Gate tunneling leakage (Ig)
- GEDL leakage (Igedl)

Figure 1 explains the various leakage components in a CMOS device

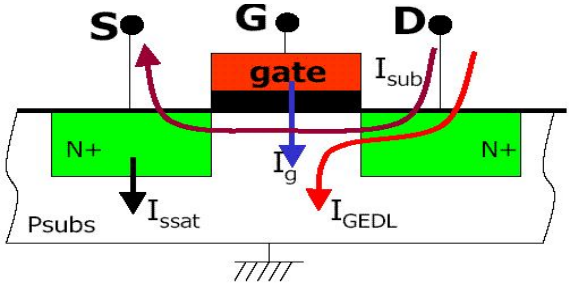

Figure 1: Different leakage in CMOS device

As the technology shrinks operating voltage decreases but the threshold voltage does not decrease proportionally, which leads to large leakage in deep submicron (DSM) designs. Starting 90nm & moving towards 14nm technologies, leakage is a major component of the total power. Figure 1a indicates the typical leakage numbers for various technology node. The

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significance of leakage number can be appreciated by noting that the leakage current alone will be 10 mA for a design with 15 million transistors in 28nm tech node.

- Device gate leakage
- Gate leakage caused by quantum tunneling effect

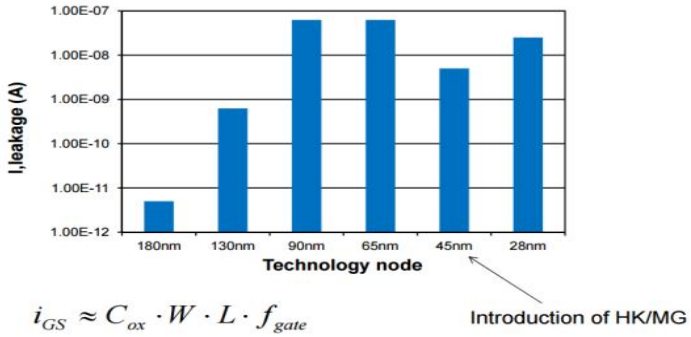

Figure 2:A typical leakage numbers in various technology nodes

Active Power can be reduced using various methods like clock gating, gate count reduction, wire length reduction, reduction of operating voltage and frequency.

Reduction of leakage power requires innovative methods and flows. The basic principle behind the leakage power saving is to split the logic domains in to multiple power domains and to remove power to those logic domains when they are not active.

The decision to gate the power to sub-domains is based on the power goals and the design requirements. The goal of power conservation mode is to power-up only the bare minimum logic required for the application and power-off the remaining logic to significantly reduce leakage current and thus power. In our design the lowest power state is known as “Shutdown” mode.

The power domain that is always powered-up is known as AON (Always ON) domain.

The leakage power saving strategy requires special cells, namely switches and guard cells to be part of the standard cell library. The switch cells are used to cut-off power to the logic gates in shutdown mode. The guard cells need to be placed on signals that cross power domains, to ensure that all inputs of powered domain are driven. In the absence of guard cells, the inputs of cells, in powered domain driven by the output of powered-off cell, will be floating. The guard cells essentially act as tie off cell in power saving mode and as buffers in the normal functional mode. The guard cells thus are buffers with an additional control signal, called PWRSV. The commonly used guard cells are TIE0 that ties a node to low (when PWRSV is high) and TIE1 that ties a node to high (when PWRSV is high). Figure 2 summarizes the power conservation architecture.

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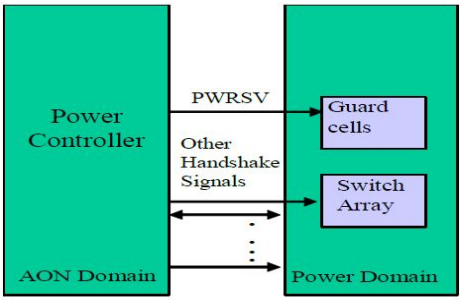

Figure 3: Interfacing of different power domains

The mobile design that needed to be ramped to production was exhibiting very high IDDQ current in the shutdown mode. The current measured in shutdown mode was 90 uA against specification limit of 8 uA. This issues would have significantly reduced the battery life and hence need to be addressed to ramp the device to production

The normal cause for high leakage currents in CMOS is contributed to floating nodes. This paper will discuss in detail about the debug cycle/method used to confirm floating node in the design. The paper also will focus on the various methods/techniques, like EMMI, available to debug silicon.

II. PROBLEM DESCRIPTION

The mobile device was meeting the power targets in functional mode but the power measured on silicon was way off the estimation in shutdown mode.

We started by analyzing the current drawn from different power domain. The device in question had two major power domains, one for memory VDDram and another for logic cells VDDcore.

A wafer was probed to measure IDDQ current in different power modes, including the shutdown mode, and the IDDQ distribution was plotted.

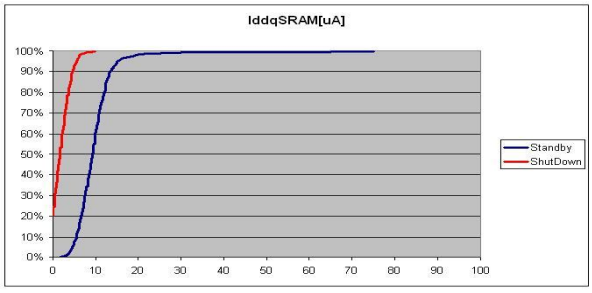

Figure 4: Plot of VDDram IDDQ

Figure 4 shows the IDDQ current variation, in RAMs, in standby mode and shutdown mode. Note that the standby mode current curve and shutdown mode current curve don't intersect. The distance between two curves indicates power saved.

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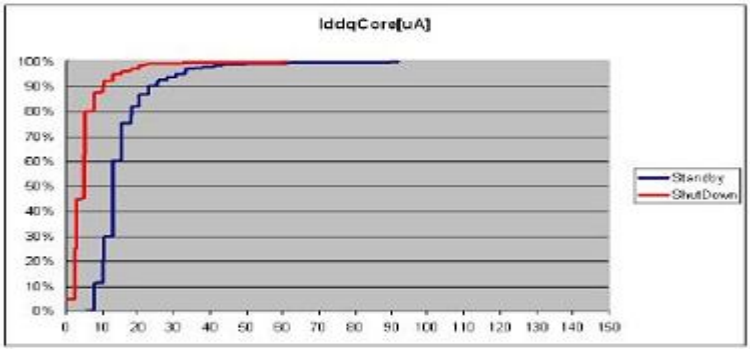

Figure 5: Plot of VDDcore IDDQ

Figure 5 shows the logic power domain IDDQ variation in standby mode and shutdown mode. Note that the tails of shutdown IDDQ curve intersects the standby IDDQ curve. The plots indicate that shutdown mode current for RAM power domain was close to estimation while those for logic power domain were way off. The analysis of the two plots concludes that the VDDcore domain only has high IDDQ issue. The plots also helped us rule out problem in switch cell because the same switch cells are used in RAM and logic power domain. Thus the problem statement was reduced to finding floating nodes within VDDcore power domain.

III. DEBUG METHODOLOGY

We now had to prove the existence of floating nodes in the design. The device was power cycled a few hundred times and the shutdown current was measured during each cycle. The random variation of current in the above experiment would indicate presence of floating node. In our case the current was constant across multiple measurements, which contradicted the above hypothesis of floating node being present in shutdown mode.

The detailed study of bench set-up indicated that the device was not coming out of a wait state. This resulted in the device always being in a known state on every power cycle, resulting in no current variation. The device required a particular transaction on the peripheral interface to come out of the wait state. On further bench experiments with the desired transaction the shutdown IDDQ current was measured. Figure 5 depicts the result of current measurement with power cycling on a single device with required transaction on the peripheral.

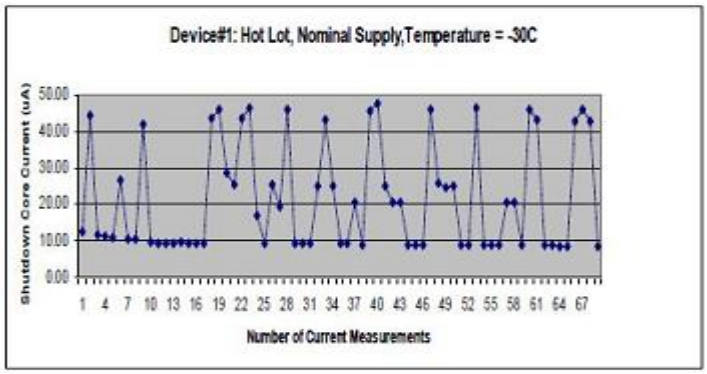

Figure 6: Shutdown IDDQ variation with power cycling

The above figure proves our hypothesis of floating nodes being the cause of high IDDQ variation in shutdown mode.

The design was analyzed for floating node in various power management modes. The net list link report confirmed no floating node. The search space thus was reduced to finding floating nodes in shutdown mode. The powered logic in shutdown mode was segregate in different sections like:

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- Switches
- Guard cells
- Always ON logic cells
- Always ON buffers

Switches were ruled out because RAM current was matching the expected results and logic Power domains also used similar switches. Always ON logic cells and always-ON buffers were also ruled out since they would have caused IDDQ issue in other power modes as well. The root-cause thus was narrowed down to guard cells. A detailed review of TIE0 guard cell circuit design revealed a discrepancy in the TIE0 Cell usage. TIE0 cell have to be placed in powered off domain. In our design 79 cell instances were placed in AON domain.

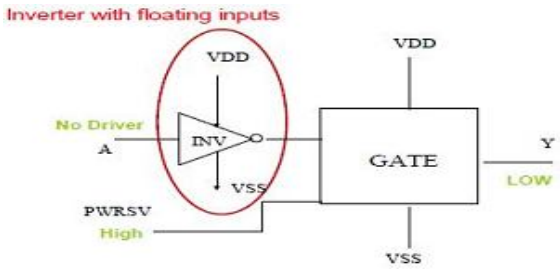

Figure 7:TIE0 guard cell transistor schematic

Figure 7 clearly shows a high IDDQ scenario in TIE0 cell when "A" input is floating and VDD power supply is present. In the actual design, the input "A" is floating during shutdown mode because it will be driven by a powered off logic.To fix this in silicon, conventional FIB (Focused Ion Beam) approach was first looked at. In DSM technology it is very difficult to FIB lower metal layers which ruled out fixing all the 79 cell instances after careful analysis of layout and design a reduced list of 12 FIB points was identified. The FIB effort was estimated as 40 hours for this reduced list. The FIB expenses are around $300/hr. The FIB option was ruled out since the cost of $12K per device was not justified given the low probability of FIB success even for a reduced fix. Hence there was a need to identify alternate methods and technology to fix this issue conclusively.

IV. RESULTS

Further bench results with and without transaction were correlated to different voltage levels at "A" input of TIE0 cells prior to shutdown mode entry. A detail analysis of software sequencing of the device with and without the transaction on peripheral revealed that 16 out of 79 TIE0 cells could have random values after power-up. The values on the inputs of 16 TIE0 inputs could also be controlled through special software patch. The Shutdown currents were measured with different known values forced on the 16-TIE0 input nodes through software patch. Figure 7 shows the IDDQ current values in shutdown mode with value of 0x0000 on these 16 TIE0 cells prior to shutdown mode entry.

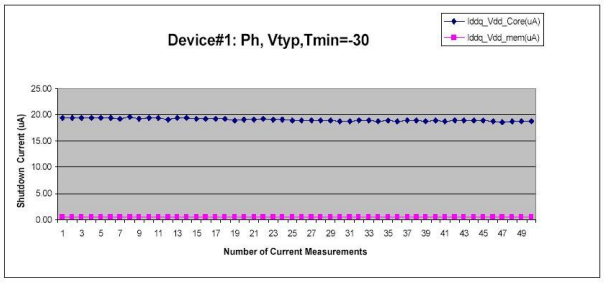

Figure 8: Shutdown IDDQ variations in power cycling with patch download for value 0x0000

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As shown the multiple current readings are now constant which provides that TIE0 cells in AON domain caused the IDDQ problem.

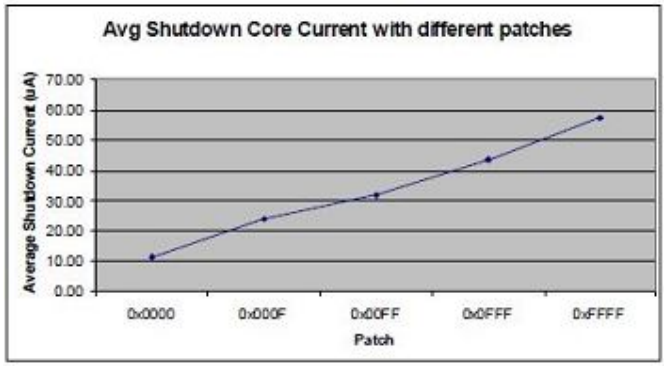

Figure 9: Shutdown IDDQ variation in power cycling with different patch download

Figure 9 shows IDDQ current variation with different values on the 16 TIE0 cells. Figure 8 shows a linear increase in IDDQ current with increase in number of TIE0 cells having "A" input as high before shutdown mode entry. This confirms the hypothesis of TIE0 to be one of the root causes of the problem. We still had to rule-out the presence of other floating nodes. To rule out any other floating node other than TIE0 silicon debug technique, EMMI was used. EMMI technology [3] is used to identify the hot-spots in the design that could indicate presence of floating nodes in silicon. EMMI technique essentially works on the principle of sensing heat emission to identify hot spots on silicon. The logic that has floating nodes will draw high current, resulting in excess power dissipation subsequently resulting in temperature increase in that region. The EMMI images thus indicate hot spots as red or yellow dots in the image. The EMMI requires currents to be in hundreds of microampere to reliably detect hot spots.

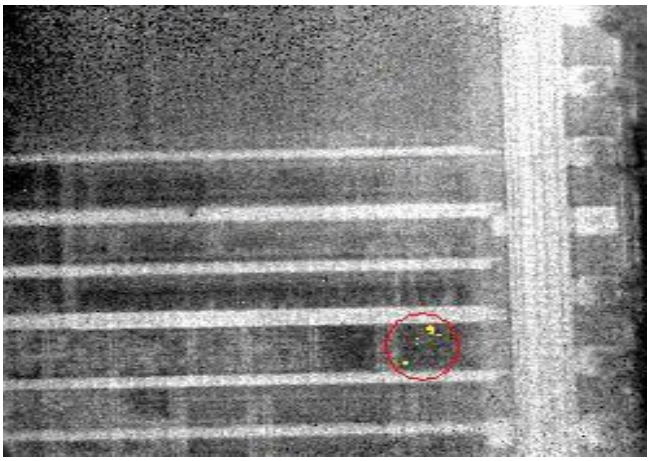

Figure 10:EMMI image at Vcore=1.3V

Figure 10 shows the EMMI images with nominal voltage applied. As seen the image does not give reliable results since the current is only about 140 uA. To get a reliable image the current had to be increased significantly. It was proposed to select devices from strong process corner and also increase the applied voltage to achieve higher IDDQ current.

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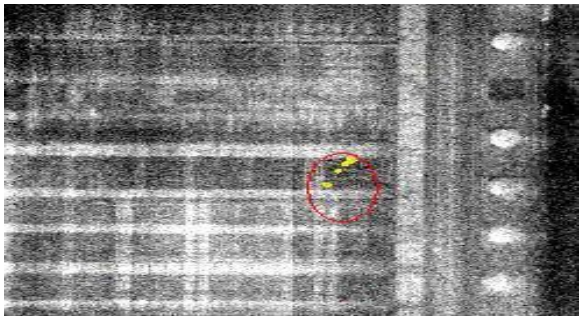

Unit-2 (999 uA@1.5V)

Figure 11:EMMI image showing hot Spot in the device at V_{core}=1.5V

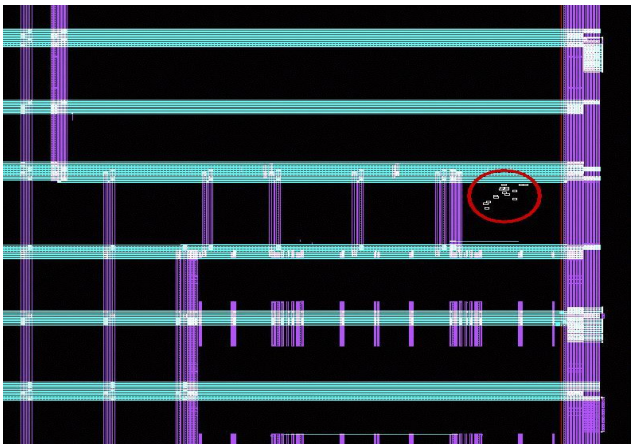

Figure 12: Layout image highlighting expected TIE0 floating nodes

Figure 12 shows the location of the same 16 TIE0 cells in layout, which were expected to be the culprits from patch, download experiment. By matching the hot spot (Figure 10) and the layout (Figure 11) it was confirmed that TIE0 was the only cause of high IDDQ current.

V. CONCLUSION

The detailed method for finding floating nodes that contributed to excess current was discussed. We also discussed methods to find floating nodes and Silicon debug techniques like EMMI to pin-out the root-cause.

VI. ACKNOWLEDGEMENT

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