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An Integrated Single Input Multi-Output DC-DC Converter with Simultaneous Buck and Boost Outputs

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ABSTRACT: Multi-port DC-DC converter topologies can be used to generate multiple DC outputs from a single DC input source. The voltage gains can be step-up and/or step-down type. This paper proposes a multi-port DC-DC converter topology which generates multiple outputs, which can step-up as well as step-down, from a single DC input. Operating modes and steady state behaviour of the proposed converter has been studied in this paper. Using MATLAB/SIMULINK (R2010a) the proposed converter topology is simulated to generate four outputs (two step-up and two step-down) from a single DC input. The control scheme used here is PIC controller (PIC16F877A) to control multiple outputs. The behaviour of the proposed converter has been verified using a laboratory prototype, which produces a step-up voltage of 30 V and a step-down voltage of 6 V from a single 15 V DC input.

KEYWORDS: Buck, Boost, Multiport Converters, Integrated Single Input Multiple Output Converter (ISIMOC),

I. INTRODUCTION

Present day power electronic systems require multiple dc outputs at different voltage levels. Auxiliary circuits are often present in addition to the main power stage, and they should be powered at low voltages, e.g., fuel cell system. Power converter architectures having multiple dc ports (input/output) are used in a wide variety of applications [1]. Typical examples include hybrid electric vehicles, dc-based nanogrids, LED drivers, stand-by power supplies, bias supplies, etc. Single-input-multi-output (SIMO) dc-dc converter stages have been utilized in many of these applications. Fig. 1 shows a representative system, where four distinct outputs (two step-up output, vo1 & vo3 and two step-down outputs, vo2 and vo4) are obtained from a single dc input using four separate power converters. In general, an N- output system requires 2N number of switches for a high efficiency synchronous implementation. For efficient operation of systems using multiple outputs, there should be proper coordination of control between each of the converters for power flow management. Fig. 2 shows the system where a single integrated architecture is used to generate the different outputs. These converters, denoted as integrated single input multi-output converter (ISIMOC) in this paper, utilizes reduced number of switches ((N + 1) switches for N outputs) compared to separate converters. The use of lower number of switches reduces the cost of the switch and its associated drivers. Also, due to its integrated architecture, all the outputs of the system are regulated using the same set of switches, and hence, the coordination control is easier.

The concept of SIMO has been reported in [2]. A class of SIMO converters, discussed in [3], use one input to create a high frequency ac which uses multiple secondary windings to generate multiple outputs (step-up or step-down depending upon the turns ratio), all of which are not well regulated. Due to magnetic coupling associated between the outputs, precise regulation of each of the outputs is difficult. For this purpose, different post-regulation schemes have been utilized on the secondary side, such as linear regulators, synchronous switch post-regulators (SSPR). Among the widely utilized non-isolated designs, Single-Inductor-Multi-Output (SIMO) DC-DC converters [4] can generate multiple DC outputs from a single DC input. The SIMO converters derive multiple outputs by multiplexing the inductor current into several paths by means of time division multiplexing. The control associated with the voltage

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regulation for each of the outputs is quite involved and different methods have been proposed in literature [5]. For Point-of-Load applications, the dynamic response of the control system needs to be sufficiently fast to provide regulated DC outputs.

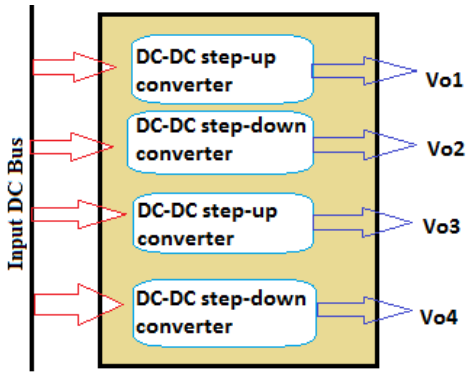

Fig. 1 Schematic of power converter architecture having four separate dc-dc converters and its outputs.

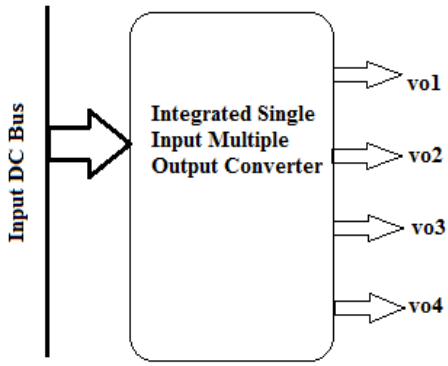

Fig. 2 Integrated single-stage architecture used to provide four dc outputs.

Many researchers have taken place in order to find other isolated multi-output dc-dc converter topologies. Resonant converter-based isolated multi-output dc-dc converter [6] has been proposed, which have ZVS and ZCS for all its switches. In general, isolated converters comprise of more circuit components, and require complex control systems. The involvement of magnetic elements in a multi-output architecture makes the system bulkier. Also, in order to achieve improved efficiencies, most of these topologies utilize synchronous switches as well as soft switching. Hence, these topologies are considered when galvanic isolation between the different ports is necessary. Different non-isolated SIMO converter designs have been reported in literature, which include use of cascaded dc-dc stages [7], time-multiplexed and current-channelized multi-output converters, etc. Among the non-isolated designs, the number of circuit elements used in cascaded stages is more, but the outputs can be precisely regulated using simple control systems. In contrast, multiplexed converters use reduced circuit components, but the control systems are associated with various constraints due to time multiplexing, operating modes, cross-regulation, etc.

This paper presents a non-isolated SIMO dc-dc architecture which can provide step-up as well as step-down outputs from a single dc input simultaneously. The proposed topology is obtained by replacing the control switch of a boost converter by series connected switches and using the resulting switch nodes to synthesize additional outputs using low-pass filter networks. The step-up as well as step-down gains achieved are same as separate boost and buck converters, respectively. However, compared to separate converters (Fig. 1), the proposed structure uses lower number of switching elements. Also, the converter has continuous currents both at the input as well as the step-down output. Hence, compared to a conventional buck or buck-boost converter, the input filter requirement is lower. The

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complementary switching operation need not have dead-time protection due to inherent protection provided by the circuit topology. The control system is exactly similar to those implemented for conventional buck and boost converter, and hence, can be easily extended to this design for precise regulation of each output. The following section describes the modification principle for the synthesis of proposed converter. The converter architecture, operating modes and the steady state analysis of the converter have been studied in section III, followed by the control strategy for the converter in section IV. Section V lists the advantages of the proposed converter. The simulation models and its results are included in section VI. The converter behaviour has been verified using a laboratory prototype, and it is shown in Section VII.

II. CIRCUIT MODIFICATION PRINCIPLE FOR THE PROPOSED CONVERTER TOPOLOGY

The realisation of the converter architecture by replacing the control switch of a boost converter is shown in fig.3. The mid-point of the half-bridge structure acts as a load point, thus providing a dual-output architecture.

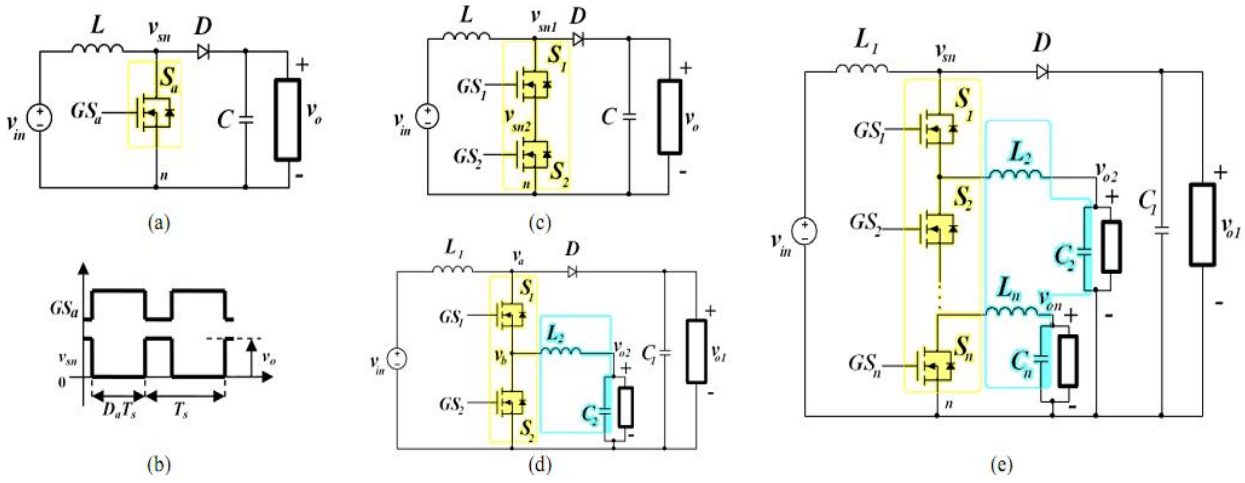

Fig. 3 Principle of circuit modification for the generation of single-input-multi-output (SIMO) dc-dc converters.

Fig. 3 (a) shows the schematic of a conventional boost converter with the single control switch S_a. The switch node voltage v_{sn} corresponding to gate signal GS_a is shown in Fig. 3(b). The switch node voltage is equal to zero when the switch S_a is turned on ($0 \le t \le D_a.T_s$) and is clamped to the boost output voltage (v_o) when the switch is off (neglecting diode drop) ($D_a.T_s \le t \le T_s$) . Fig. 3 (c) shows the boost converter circuit when the switch S_a is replaced by two series connected switches S_1 and S_2. For boost operation (D_a interval), both the switches need to be turned on at the same time. The resulting circuit has been shown in Fig.3 (d), where L_2 and C_2 are used in the low pass filter. Thus the proposed modification results in boost converter as well as the buck converter being integrated in a single topology. Hence, in this paper this converter is regarded as integrated single input multi output converter (ISIMOC) and the behavioural characteristic of the converter has been studied. The same set of switches S_1 and S_2 are used to regulate both the outputs. The proposed circuit modification principle can be extended to achieve multiple dc outputs by replacing the boost converter control switch S_a with N-number of series connected switches and filter networks. Fig. 3(e) shows the schematic of the generation of N multiple outputs. This concept leads to the use of only (N + 1) switches for N-outputs, compared to 2N switches when individual converters are used. Thus, compared to separate converters, this topology saves the total number of semiconductor devices (including active and passive switches).

III. PROPOSED CONVERTER TOPOLOGY

The schematic of the converter, proposed in this paper, is shown in Fig. 4. From a single DC input (v_{in}), this three-port converter provides step-up as well as step-down operations at its two output terminals v_{o1} and v_{o2}, respectively. The converter architecture has been derived by replacing the controllable switch of a conventional boost converter by the

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two bidirectional switches Q_1 and Q_2, along with the low pass filter comprising of inductor L_2 and capacitor C_2, which provides the additional step-down output port.

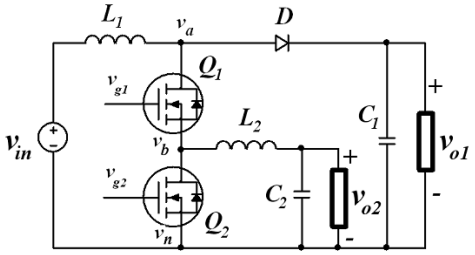

Fig. 4 Schematic of the proposed integrated single input dual output converter.

A. Steady State Operation of the Converter

The paper considers continuous conduction mode of operation (CCM) . The converter has been implemented using two bidirectional switches S_1 and S_2. These two switches would result in four possible operating states, three of which are distinct and thus results in three different switching intervals of the converter. These intervals are discussed in the following sections.

1) Interval I (t1 - t2): Both S1 and S2 are ON:

Interval I occurs when both the switches S_1 and S_2 are in the ON condition. This mode of operation is equivalent to the controllable switch of a conventional boost converter being turned ON. The diode D is reverse biased during this interval. The inductor current i_{L1} builds up during this interval, while the buck inductor current i_{L2} freewheels through the switch S_2. Fig. 5(a) shows the equivalent circuit of the converter at interval I. With respect to the waveforms shown in Fig. and considering the DC loads R_{o1} and R_{o2} at the step-up and step- down terminals respectively, for a time $D_1.T_s$, (where T_s = switching period). The time duration for Interval I operation is defined by duty ratio D_1. The equations governing this mode of operation are shown below:

$$V_{L1} = V_{in} \quad (1)$$

$$V_{L2} = V_{o2} \quad (2)$$

$$i_{C1} = -\frac{Vo1}{Ro1} \quad (3)$$

$$i_{C2} = i_{L2} - \frac{Vo2}{Ro2} \quad (4)$$

2) Interval II (to - t1 and t2 - t3): S1 is ON and S2 is OFF:

Interval II occurs when the switch S_1 is ON and S_2 is OFF. The inductor current i_{L1} is distributed into two components- one flowing through the diode D and the other portion is equal to the buck inductor current i_{L2}. In this interval, the step-down converter draws energy from the source. The equivalent circuit diagram of the converter in this mode has been shown in Fig. 5(b). Unlike conventional boost converter, the diode current i_D is equal to the difference between the inductor currents i_{L1} and i_{L2}, and hence its magnitude decides whether the converter operates in CCM. The switch node voltage (v_a) is equal to the step-up output voltage V_{o1}. The time duration for Interval II operation is defined to have a duty cycle of D_2 during this interval,

$$V_{L1} = V_{in} - V_{o1} \quad (5)$$

$$V_{L2} = V_{o1} - V_{o2} \quad (6)$$

$$i_{C1} = i_{L1} - i_{L2} - \frac{Vo1}{Ro1} \quad (7)$$

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$$i_{C2} = i_{L2} - \frac{Vo2}{Ro2} \quad (8)$$

3) Interval III (t3 - t4): Both S1 and S2 are OFF:

Interval III occurs when both the switches S_1 and S_2 are in the OFF condition. During this time the inductor current iL2 freewheels through the anti-parallel diode of the bidirectional switch S2 (if S2 is not being gated). This interval is thus analogous to freewheel period associated with conventional buck converters, either the lower switch conducts in synchronous switching scheme or the diode conducts. The diode D conducts the inductor current iL1. Hence, both the inductors give out their energy to their respective outputs. Fig.5(c) shows the equivalent circuit diagram. During this interval

$$V_{L1} = V_{in} - V_{o1} \quad (9)$$

$$V_{L2} = - V_{o2} \quad (10)$$

$$i_{C1} = i_{L1} - \frac{Vo1}{Ro1} \quad (11)$$

$$i_{C2} = i_{L2} - \frac{Vo2}{Ro2} \quad (12)$$

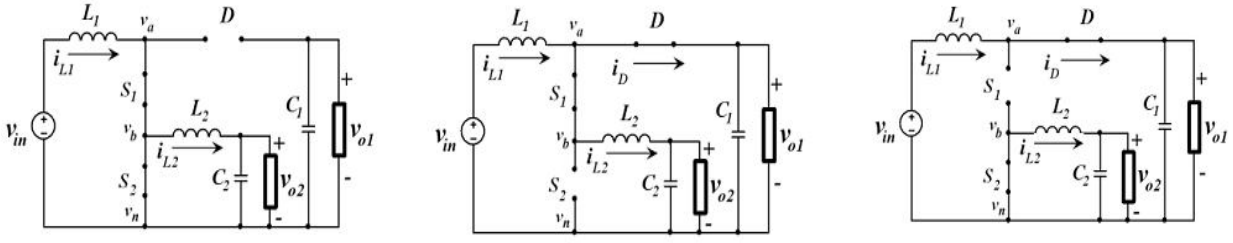

Fig.5 shows the equivalent circuit of the proposed converter at different operating intervals. The figure shows (a) interval I , (b) interval II and (c) interval III.

Fig. 6 shows typical waveforms of the inductor currents i_{L1}, i_{L2}, and the switch node voltages v_a and v_b at different operating modes. The switching strategy makes the converter to operate in the interval sequence (III), (II), (I), (II), (III) during each period. It is important to note that Mode III in Fig. 6 shows GS_1 and GS_2 being turned off. The waveforms would be same if during Mode III; GS_2 is switched on, thus resulting in synchronous switching operation.

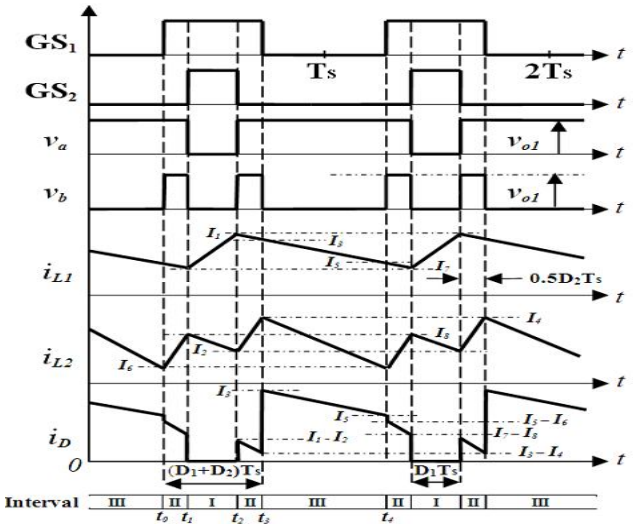

Fig. 6 shows typical waveforms of the switch node voltages, the inductor and the diode currents. The duty cycles are D_1 and D_2.

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B. Steady State Analysis of the Converter

1) Voltage conversion ratio:

For the purpose of analysis, small ripple approximation for the inductor currents and capacitor voltages has been assumed.

Thus the expressions for the voltage conversions can be derived from equations (1)-(12), as follows:

For the inductor L_1,

$$V_{in} * D_1 + (V_{in} - V_{o1}) * (1 - D_1) = 0$$

Hence,

$$\frac{Vo1}{Vin} = \frac{1}{(1-D1)} \quad (13)$$

Similarly, for inductor L_2,

$$(V_{o1} - V_{o2}) * D_2 + (- V_{o2}) * (1-D_2) = 0$$

Hence,

$$\frac{Vo2}{Vo1} = D_2 \quad (14)$$

Thus,

$$\frac{Vo2}{Vin} = \frac{Vo2}{Vo1} * \frac{Vo1}{Vin} = \frac{D2}{(1-D1)} \quad (15)$$

From equations (13) and (15), it can be seen that the two dc outputs of the converter can be regulated using the two control variables D_1 and D_2. These duty cycles are defined as the time duration for intervals I and II, respectively. The step-up output depends upon the interval when both the switches are turned "ON" simultaneously (dependent upon duty D_1) while, the step-down output is regulated solely using the switch Q_1, when Q_2 is "OFF" (dependent upon both D_1 and D_2). The step-up output voltage, thus, effectively acts as input to the step-down operation.

2) Range of output voltages:

The previous section describes the duty cycles that control both step-up as well as the step-down voltages. The duty cycles D_1 and D_2, for proper operation, should satisfy the condition (16),

$$D_1 + D_2 \leq 1 \quad (16)$$

For any particular value of the duty cycle D_1, the step-down gain varies within the range:

$$0 \leq \frac{Vo2}{Vin} \leq 1 \quad (17)$$

Thus, the ISIMOC can provide step-down output ranges varying from zero to the input voltage. Compared to a conventional

Buck converter, the ISIMOC can provide wide step-down outputs at acceptable duty ratios of switches. This is because the step down output depends upon both D_1 and D_2, instead of only one duty cycle as in the case of a buck converter. Similarly, the step-up gain varies between:

$$1 \leq \frac{Vo1}{Vin} \leq \frac{1}{(1-D1)} \quad (18)$$

Thus, the ISIMOC preserves the qualities of both buck as well as boost converters in an integrated architecture.

3) Input Current Expression:

Assuming the input current to be i_{in} ($=i_{L1}$) and the output currents i_{o1} and i_{o2}, the power balance equation for the ISIMOC, neglecting any loss component, can be written as:

$$v_{in} * i_{in} = v_{o1} * i_{o1} + v_{o2} * i_{o2}$$

Or,

$$i_{in} = \underbrace{\frac{vo1}{vin} * i_{o1}}_{\text{STEP-UP}} + \underbrace{\frac{vo2}{vin} * i_{o2}}_{\text{STEP-DOWN COMPONENT}} \quad (19)$$

The first component denotes the step-up component and the second one denotes the step-down component. Thus, compared to conventional boost converters, the input current for the ISIMOC is higher, due to the additional power drawn by the step-down load.

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IV. CONTROL STRATEGY

In this paper, a simple control scheme has been described, which directly utilizes the control structure of conventional buck as well as boost converters with minimum changes. Alternate control architectures, resulting in higher efficiencies are possible; but they would require a different PWM control structures compared to those used for separate converters. One possible scheme is to use synchronous switching (S_2 is turned on during Interval III). For the ISIMOC, the modulating signals (v_{GS1_mod} and v_{GS2_mod} of Fig. (7)are compared to the same carrier, with switch S_1 being provided with PWM signals of duty (D_1 + D_2) and S_2 being provided with a signal of duty D_1. The main constraint regarding the control is given by relation (16). Fig. 7 shows the reference control signals and the corresponding duty cycles for the ISIMOC. Fig. 8 shows a simple analog implementation schematic for generation of control signals for the converter. The voltage divider schematic shown in Fig 8 ensures that the relation (16) is satisfied. The control signals are shown in Fig.7.

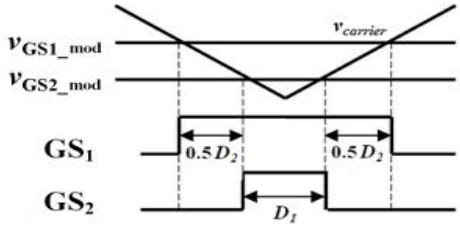

Fig. 7 shows reference control signals for generation of PWM for ISIMOC.

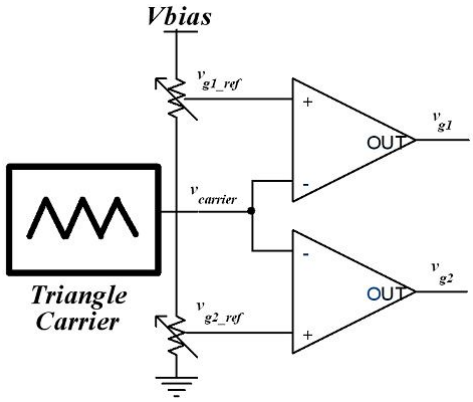

Fig. 8 Typical control schematic for generation of control signals for the proposed converter.

V. SIMULATION RESULTS

The first section describes about the software implementation of the basic topology - "Integrated Single Input Dual Output Converter". The simulation results include simulation model and its corresponding waveforms of the basic converter topology. The second section gives the simulation results of the modified converter topology.

A) Simulation Results of the Proposed Converter :

The proposed single input multiple output converters has been simulated using the MATLAB/SIMULINK R2010a.The simulated results justifies the behaviour of the converter. The results shows that the proposed converter can generate step up as well as step down out-puts simultaneously with various duty cycles. The design parameters and specifications are shown in table I.

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TABLE I
PARAMETERS AND SPECIFICATIONS.

Sl no.	Parameters	Attributes
1	Input voltage V_{in}	12 V
2	Step-up output voltage V_{o1}	Range : 20- 30 V
3	Step-down output voltage V_{o2}	Range : 4 – 8 V
4	Switching frequency	100 KHz
5	Inductors $L_1 = L_2$	15.3 µH
6	Capacitors $C_1 = C_2$	363 µF

1) Simulation Models and Waveforms :

The Integrated single input multiple output converter works for an input voltage of 12 V DC and generates two output voltages simultaneously. One output with a step-up voltage in the range of 20 to 30 V and other with a step-down voltage in the range of 4 to 8 V. The pulses to the switch MOSFET is generated using PWM pulse generator. The fig.7 shows the PWM Pulse generation circuit. The two pulses generated have a switching frequency of 100 KHz and have a variable duty cycles. By varying the duty cycles a wide range of step-up as well as step-down voltage gains can be achieved.

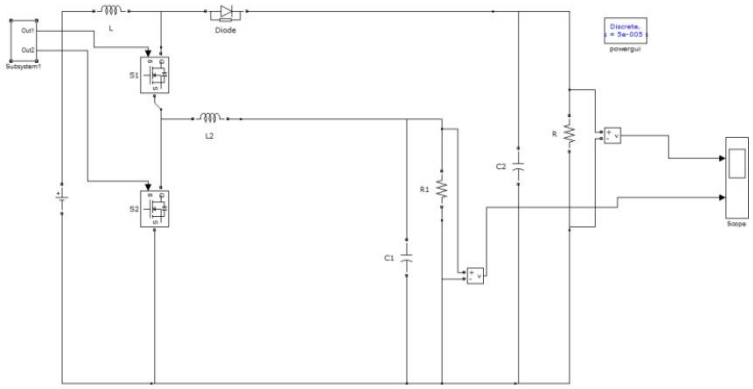

Fig. 8 Simulink Model of the Converter.

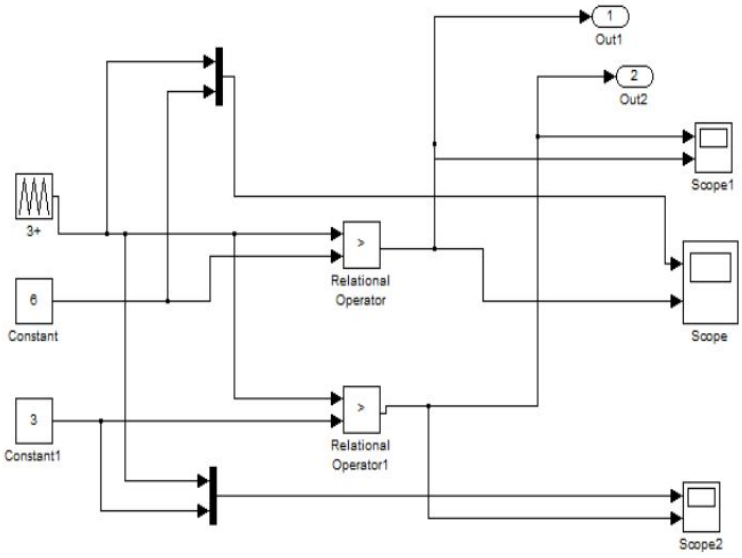

Fig.9 PWM Generation Circuit

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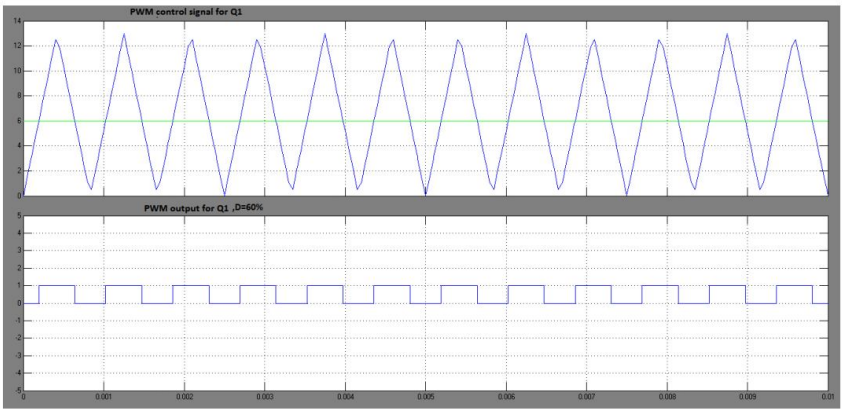

Fig. 10 PWM Output for switch S_1

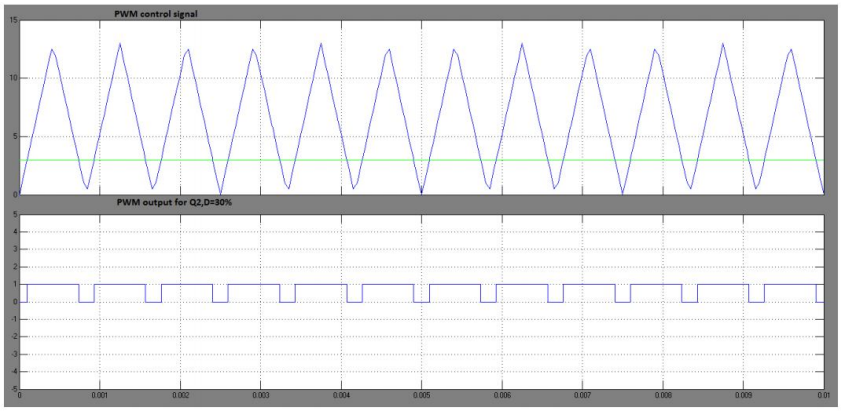

Fig.11 PWM Output for switch S_2

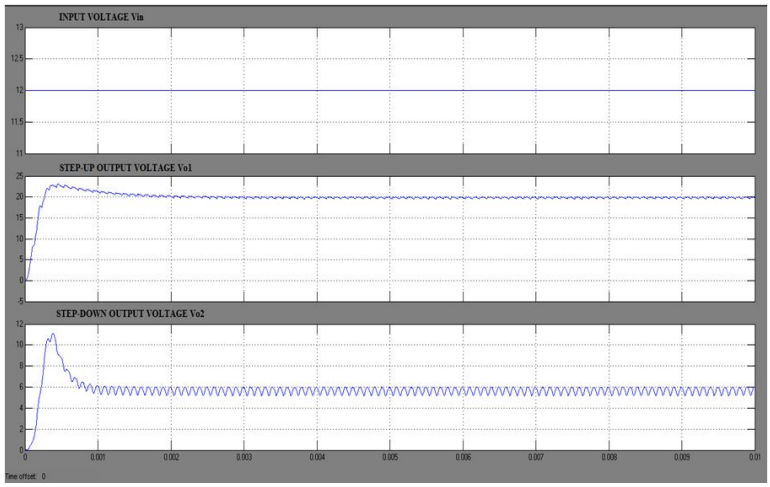

Fig. 12 Output Voltage

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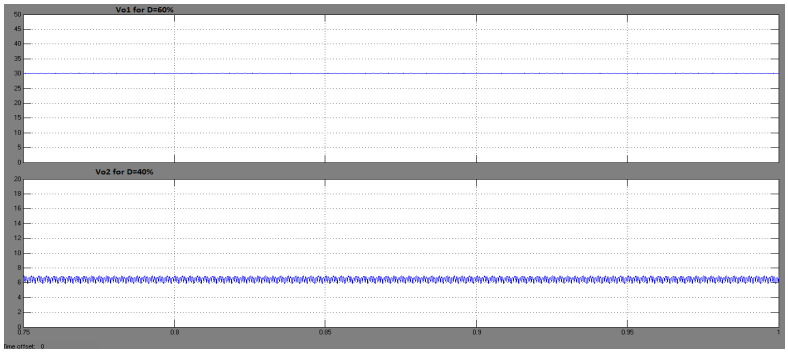

Fig.13 Output Voltage for a duty ratio of D_1 =60%, D_2 =40%, V_{o1} =30V, V_{o2} =6 V.

B) Modified Simulation Model :

The converter architecture has been derived by replacing the controllable switch of a conventional boost converter by the two bidirectional switches Q1 and Q2, along with the low pass filter comprising of inductor L2 and capacitor C2, which provides the additional step-down output port. This concept of replacing the single switch of the boost converter with two switches in series can be extended to N- number of switches in order to generate multiple outputs. Thus a modified circuit is obtained with four switches which results in four outputs, having two step-up outputs and two step-down outputs. The output voltages are in the range of 0 to 30 V. The output voltages thus obtained for an input of 12 V DC supply are, a step-up voltage of 30V and 15V, and step-down voltage of 8V and 4V. The modified circuit with four outputs is shown in fig.

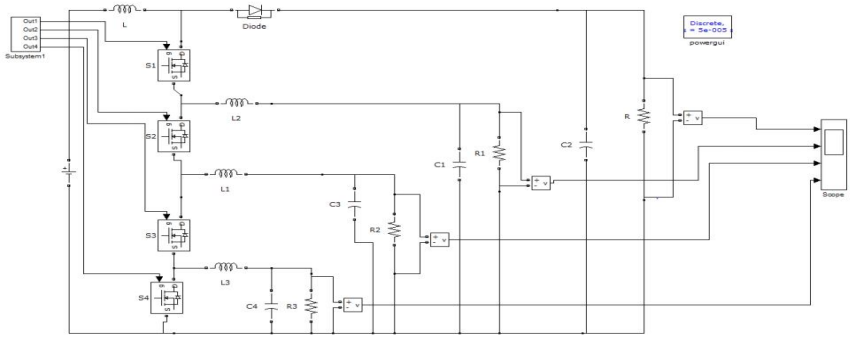

Fig. 14 Modified Integrated Single Input Multiple Output Converter

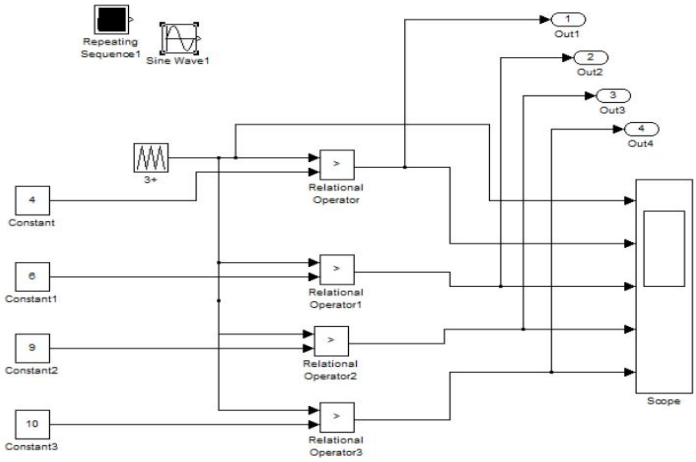

Fig.15 PWM generation circuit for the modified converter.

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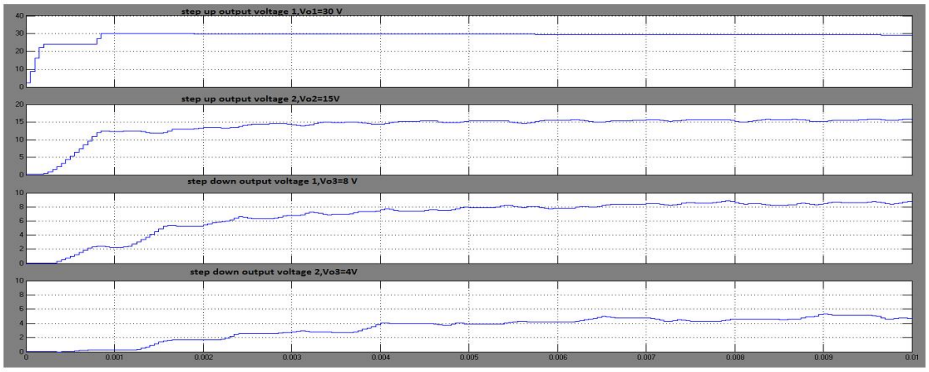

Fig.16 Output voltages of Modified Converter. V_{o1} =30V, V_{o2}=15V, V_{o3} =8V, V_{o4}=4V (where V_{o1} &V_{o2} are step-up voltages and V_{o3} &V_{o4} are step-down voltages)

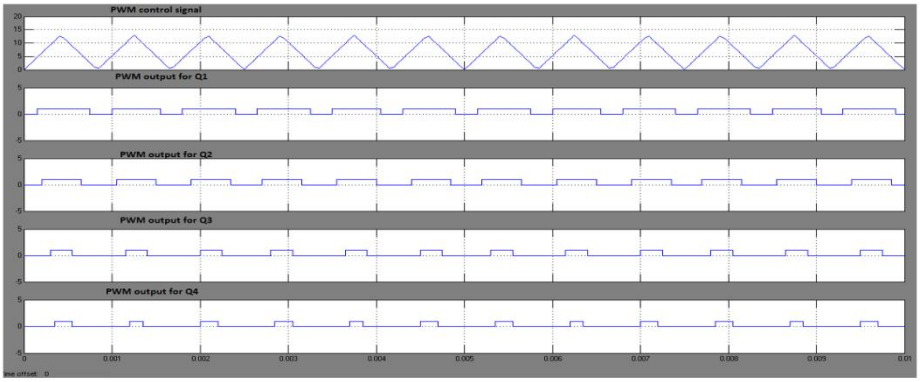

Fig. 17 PWM output pulses for switches Q_1, Q_2, Q_3, & Q_4

VI. EXPERIMENTAL RESULTS

The experimental setup for proposed Integrated Single Input Multiple Output converter (ISIMOC) has been developed as shown in fig.18. The hardware includes a main circuit, control circuit and a driver circuit. Main circuit includes two MOSFET switches S_1 & S_2, two inductors L_1 & L_2 and two capacitors C_1 & C_2. PIC16F877A is used as the control circuit for the two MOSFET switches. It generates the respective pulses for the production of control signals with a less amplitude of about 5 V. The driver circuit TLP250 which is an opto-coupler boost the 5 V switching pulses to about 15 V amplitude which drives the MOSFET switches. The input to the main circuit is about 15 V DC. It generates a step-up output voltage of about 30-35 V range and a step-down output voltage in the range of 6-9 V. Fig.19 shows the output results of the converter, which indicates that the behaviour of the proposed Integrated Single Input Multi Output is actually feasible with good accuracy.

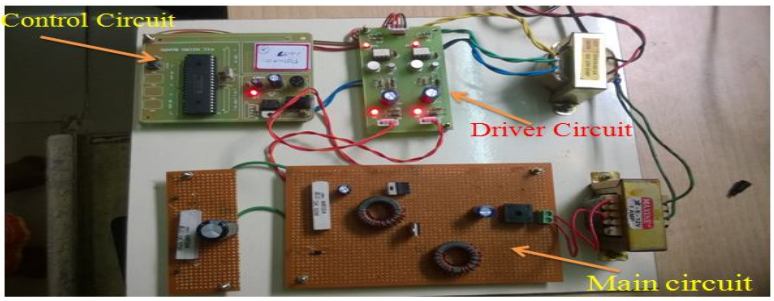

Fig.18 shows the experimental set-up for the proposed ISIMOC converter

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TABLE III
HARDWARE COMPONENTS AND SPECIFICATIONS.

Sl no.	Components	Specifications
1	MOSFET	IRF840
2	Inductors L_1=L_2	20µH
3	Capacitors C_1 , C_2	1000 µF,470 µF
4	Switching frequency	100 KHz
5	Controller	PIC16F877A
6	IC-Optocoupler	TLP250

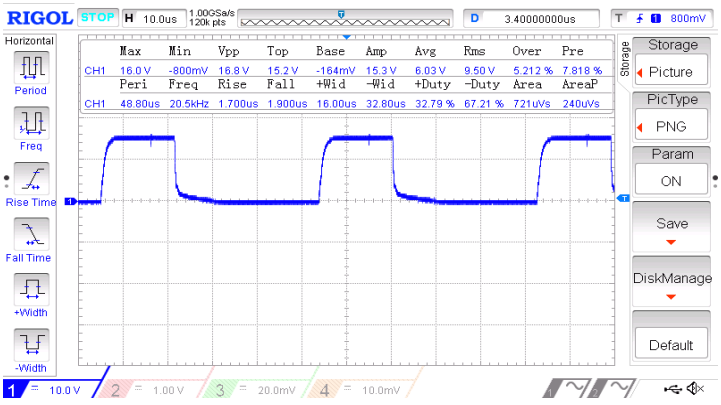

Fig.19 shows the switching pulse for switch S_1.

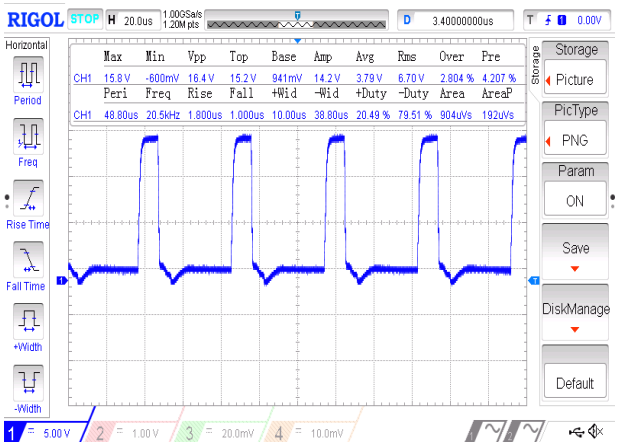

Fig.20 shows the switching pulse for switch S_2.

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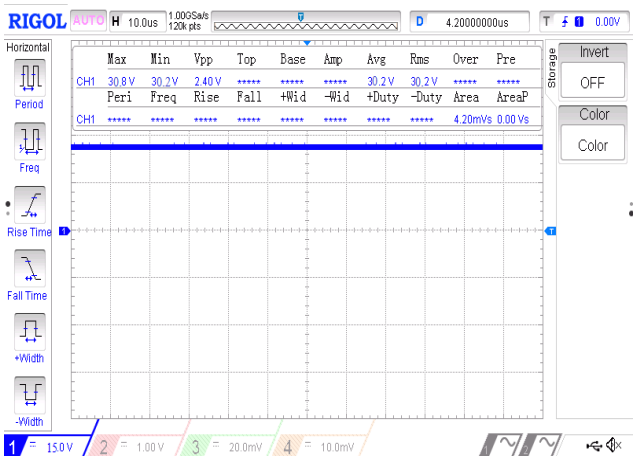

Fig. 21 shows the step-up output voltage V_{o1}.

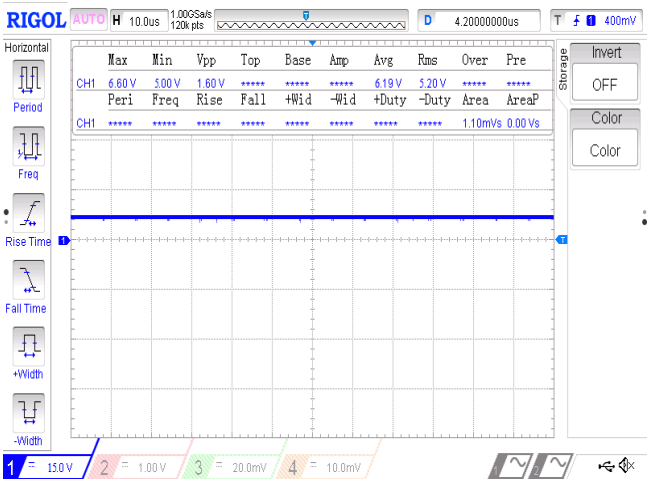

Fig. 22 shows the step-down output voltage V_{o2}.

VII. CONCLUSION

This paper proposed an Integrated Single Input multi-output dc-dc converter topology with simultaneous step-down as well as step-up outputs. In contrast to a conventional buck converter, the proposed converter has continuous input as well as the step-down output current. Analysis and characterization of the different modes of operation of the converter is done. The merits of the converter with respect to shoot-through protection, lesser Bill-of-Material and wider output ranges have been discussed. The converter behaviour has been verified using a simulation as well as experimental prototype.

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