ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 10, October 2014

Application of Single Electron Threshold Logic based Device: - A case study

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ABSTRACT: The very high density of integration and ultra-low power consumption characteristics has given the Single electron devices promising capabilities to replace CMOS transistors in some applications. There are also alternative logic design styles, such as threshold logic, that may be more suitable and also more powerful for novel technologies such as single electron technology. In this paper, we investigate single electron threshold logic gate implementation of some logic circuits, in which the Boolean logic values are encoded as absence or presence of one electron. We present a control unit for a chemical process. Computer based realization of the control unit is performed using SIMON simulation tool. The performance of the simulated model is studied with some sample data and found satisfactory thereby establishing the feasibility of using single electron threshold logic based devices for high future high density low power VLSI/ULSI circuits.

KEYWORDS: Coulomb blockade, Single electron tunnelling, Threshold logic gate, Tunnel junction.

I.INTRODUCTION

Single electronics have attracted much attention because of their very low power consumption and ultra small size [1]. The ever-decreasing size and the corresponding increase in the density of transistors facilitated improvements in semiconductor based designs. The MOS technology will presumably be continued for some more years by the well-known scaling of structure geometry [2]. There have been reports suggesting that the MOS transistor cannot shrunk beyond certain limits [3]. Single Electronics is a possible successor technology with greater scaling potential. The Single Electron Tunneling (SET) technology is the most promising future technology to meet the required increase in density, performance and decrease in power dissipation [4, 5]. The main device of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [5]. The operation of the tunnel junction is based on the Coulomb blockade [6]; the tunneling of an electron into an ultra small conductive island is inhibited by the charging energy. There are many reports on SET transistors using metals, GaAs, and Si [7]. Single-electron memories using metals and Si have also been widely investigated [7]. Any function can be computed using a network of conventional Boolean gates such as AND, OR, NAND and NOR logic gates. However, there are alternative logic design styles, such as threshold gate based logic, that may be more suitable for novel technologies such as single electron tunnelling technology. Threshold gates are fundamentally more powerful than the conventional Boolean gates. Moreover a number of theoretical investigations suggest that threshold logic may be a promising design approach.

In this paper, we first briefly discuss the basic physics of single electron devices. Some single electron device based threshold logic gates like OR, AND and Buffer/NOT are described. A control unit for a chemical process is described, designed and implemented with Single electron device based threshold logic gates. Analysis of the proposed control unit and results are also discussed.

II.THE BASIC PHYSICS

The basic component of single electronics is the tunnel junction. A tunnel junction can be considered as two conductors separated by a thin layer of insulating material as shown in Fig. 1. A tunnel junction can be thought of as a leaky capacitor [8] which is characterised by a capacitance C_j and a resistance R_j, each of which depends on the physical size of the tunnel junction and the thickness of the insulator. The transport of electron through a tunnel junction is called tunneling.

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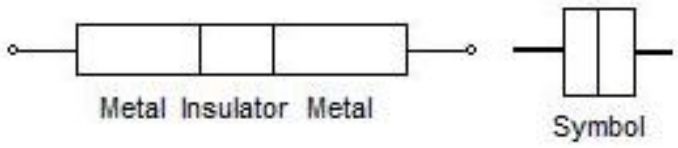

Fig. 1 Schematic representation of tunnel junction

Electrons are considered to tunnel through a tunnel junction one after another [8, 9]. Even only one electron tunnelling may produce a potential e/C across the tunnel junction (where C is total capacitance and e = 1.602 x 10^{-19} C). The threshold voltage which is the voltage needed across the tunnel junction for an electron to tunnel through the junction is called the critical voltage (V_c) and is given by [8]:

$$V_c = \frac{e}{2(C_e + C_j)} \tag{1}$$

In (1), C_j is the junction capacitance and C_e is the equivalent capacitance for remainder circuit as viewed from the tunnel junction's perspective. Tunnel event will occur across the tunnel junction if and only if the voltage *Vj* across the tunnel junction is greater than or equal to V_c i.e $|V_j| \geq V_c$, otherwise the tunnel event cannot occur. The circuit will be in stable state if $|V_j| < V_c$.

A Threshold Logic Gate

Threshold logic gates (TLG) are devices which can compute any linearly separable Boolean functions given by [8].

$$Y = \text{sgn}\{F(X)\} = \begin{cases} 0 & if \quad F(X) < 0 \\ 1 & if \quad F(X) \geq 0 \end{cases} \tag{2}$$

and

$$F(X) = \sum_{i=1}^{n} w_i \, x_i - \psi \tag{3}$$

Where ψ is a threshold value, x_i is the i^{th} input and w_i is the corresponding integer weight. If the weighted sum of inputs $\sum_{i=1}^{n} w_i x_i$ is greater than or equal to ψ, the gate produces logic 1 at the output; otherwise output will be logic 0.

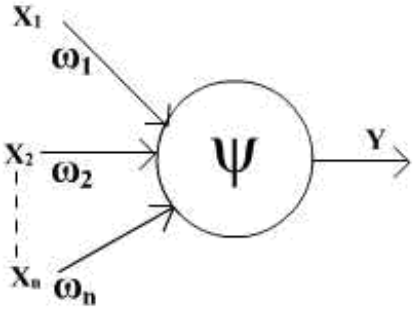

Fig. 2(a) TLG Gate symbol

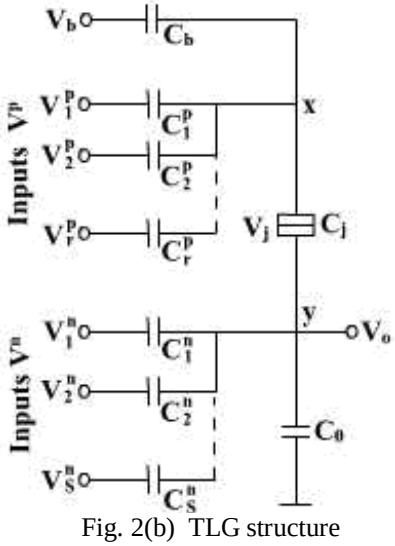

Fig. 2(b) TLG structure

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The TLG gate symbol and structure of *n* input TLG are depicted in Figs 2(a) and 2(b). The input voltages V^p weighted by their input capacitances C^p are added to V_j and the input voltages V^n weighted by their input capacitances C^n are subtracted from V_j. The critical voltage V_c of the tunnel junction which can be adjusted by the bias voltage V_b weighted by C_b acts as the threshold value. The function F(X) for the circuit is given by

$$F(X) = C_{\Sigma}^{n} \sum_{k=1}^{r} C_K^P V_K^P - C_{\Sigma}^{P} \sum_{l=1}^{S} C_l^n V_l^n - \psi \quad (4)$$

$$\psi = \frac{1}{2}\left(C_{\Sigma}^{p} + C_{\Sigma}^{n}\right)e - C_{\Sigma}^{n} C_b V_b \quad (5)$$

Where $C_{\Sigma}^{P} = C_b + \sum_{K=1}^{r} C_K^p$ and $C_{\Sigma}^{n} = C_o + \sum_{l=1}^{n} C_l^n$. The generic threshold gate describe here can be used to implement any logic function. To prevent loading effect as well as to maintain correct voltage levels, SET buffer/inverting are connected at the output of the TLG (10). The circuit of such buffer/inverter is shown in Fig. 3.

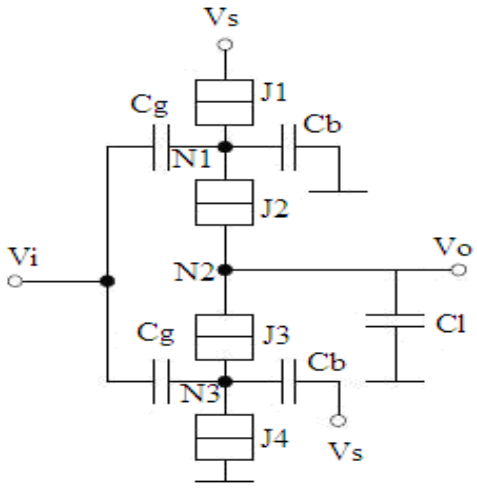

Fig. 3 SET Buffer/Inverter circuit

III. DESIGN OF THE PROCESS CONTROLLER

A block diagram of a process controller which is taken from Ref. 10 is shown in figure 4 for convenience of discussion. Temperature and pressure are the input variables. The output variables are the signals to the heater, valve and alarm.

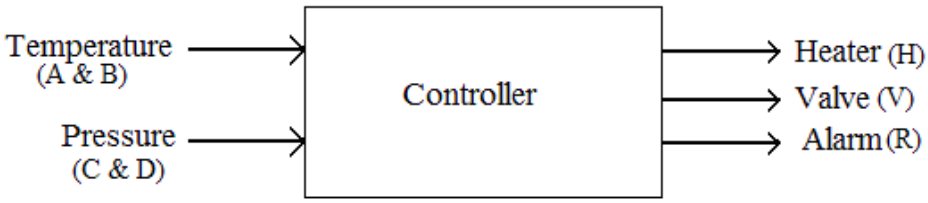

Fig. 4 Block diagram of Process Controller

The control is exercised by switching on or off a heater and by opening or closing a valve. The control rules are given below [10]:

1. If temperature and pressure are in the normal range, switch off the heater and close the valve.
2. If the temperature is normal, switch off the heater. Open the valve if the pressure is above normal and close it if it is below normal.

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3. If the pressure is normal, close the valve. Turn on the heater if the temperature is below normal and turn it off if the temperature is above normal.
4. If the pressure is above normal and the temperature is below normal open the valve and turn off the heater.
5. If the temperature is above normal and the pressure is below normal, turn off the heater and close the valve.
6. If both temperature and pressure are above or below normal, ring an alarm and shut down the plant.

The temperature and pressure variables are coded as shown in table 1 and the output variables are coded as shown in table 2.

Table 1: Temperature and Pressure Variables

Temperature			Pressure		
A	B	Condition	C	D	Condition
0	0	Normal range	0	0	Normal range
0	1	Below normal	0	1	Below normal
1	0	Above normal	1	0	Above normal
1	1	Impossible	1	1	Impossible

Table 2: Output variables

Signal to Heater		Signal to valve		Signal to Alarm	
H	Remarks	V	Remarks	R	Remarks
0	Turn off	0	Close valve	0	Off
1	Turn On	1	Open valve	1	on

The truth table for the controller to be designed is shown in Table 3.

Table 3: Truth Table of the Controller

Input				Output		
A	B	C	D	H	V	R
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	ϕ	ϕ	ϕ
0	1	0	0	1	0	0
0	1	0	1	ϕ	ϕ	1
0	1	1	0	0	1	0
0	1	1	1	ϕ	ϕ	ϕ
1	0	0	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	ϕ	ϕ	1
1	0	1	1	ϕ	ϕ	ϕ
1	1	0	0	ϕ	ϕ	ϕ
1	1	0	1	ϕ	ϕ	ϕ
1	1	1	0	ϕ	ϕ	ϕ

The logic expressions for implementation of the control unit are $H = B.\overline{C}$, $V = C$ and $R = A.C + B.D$, The design is done following conventional digital system design scheme which can be found in Ref. 10 and hence not detailed here. Here, we are interested in the single-electron threshold logic based implementation of the controller. The logic circuit of the process controller is shown in Fig 5.

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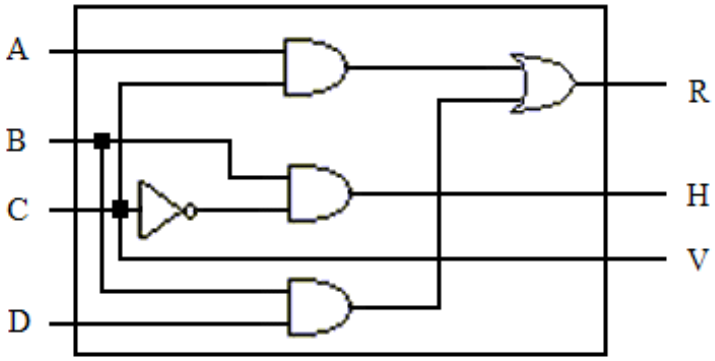

Fig. 5 Logic Circuit of the Process Controller

IV.DESIGN OF SET BASED THRESHOLD LOGIC GATES

The threshold equations for 2-input AND and 2-input OR gates can be written as

Y = AND(a,b) = sgn{a+b - 2} (6)
Y = OR(a,b) = sgn{a+b-1} (7)

There may be variations in circuit parameters in any circuit. To maximize robustness for such variations in parameter values, the threshold value ψ =I (i being an integer) is replaced by the average of the interval (i.e ψ =i-1/2) [8] and (6) and (7) are written as

Y = AND(a,b) = sgn{a+b-1.5} (8)
Y = OR(a,b) = sgn{a+b -0.5} (9)

Both 2-input AND and 2-input OR gates have the same LTG structure but they will have different circuit parameter values. The structure of 2-input AND/OR gate is shown below.

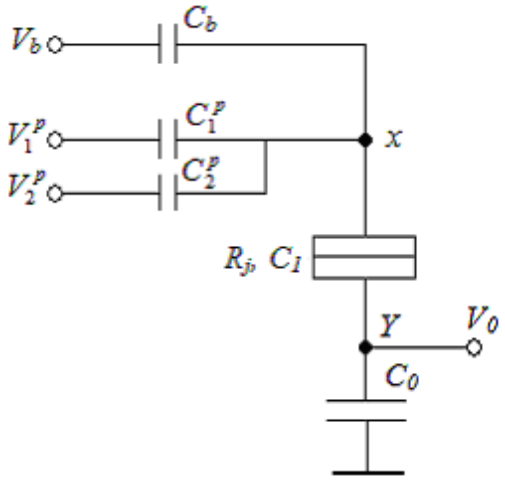

Fig. 5. Structure of 2-input AND/OR Gate

When a buffer is connected, we need to reverse the positively and negatively weighted inputs in the logic function accordingly. The structure of buffered 2-input AND/OR gate is shown in Fig. 6.

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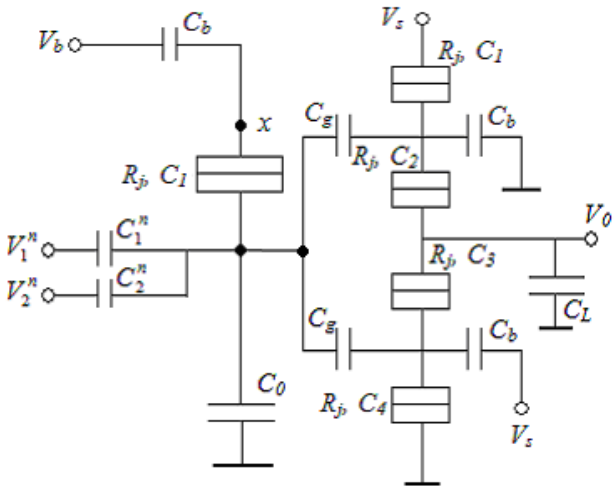

Fig.6 Structure of buffered 2-input AND/OR Gate

The threshold equation of the buffered gates can be written as

$$Y = AND(a,b) = sgn\{-a-b+1.5\} \quad (10)$$
$$Y = OR(a,b) = sgn\{-a-b+0.5\} \quad (11)$$

Assuming logic '0'=0 V, logic'1'=16mV, Rj=10^5 ohm and Cj=0.1aF, the values of the circuit parameter are designed for 2-input AND gate from equations (4), (5) and (10) and for the OR gate from equations (4), (5) and (11), respectively. The values are given in Table II. For the buffer/inverter, circuit parameters values are taken from Ref. 7.

Table 4: Parameter values of LTG gates

GATE	PARAMETER VALUES
BUFFER/INVERTER	V_s = 16mV , Cg=0.5aF, C_1 = C_4 = 0.1aF, C_2 = C_3 = 0.5aF, Cb=4.25aF, C_l = 9aF, Rj=10^5 ohm
AND	C_b=13.2 aF, C_o=8 aF, C_1^n=C_2^n= 0.5 aF, V_b=16mV, Rj=10^5 ohm, Cj=0.1aF
OR	C_b=11.7 aF, C_o=8 aF, C_1^n=C_2^n= 0.5 aF, V_b=16mV, Rj=10^5 ohm, Cj=0.1aF

V. RESULT AND DISCUSSION

The proposed process control unit is verified by simulation using SIMON [11]. The complete circuit of Single Electron TLG based Process control circuit is given in Fig. 7.

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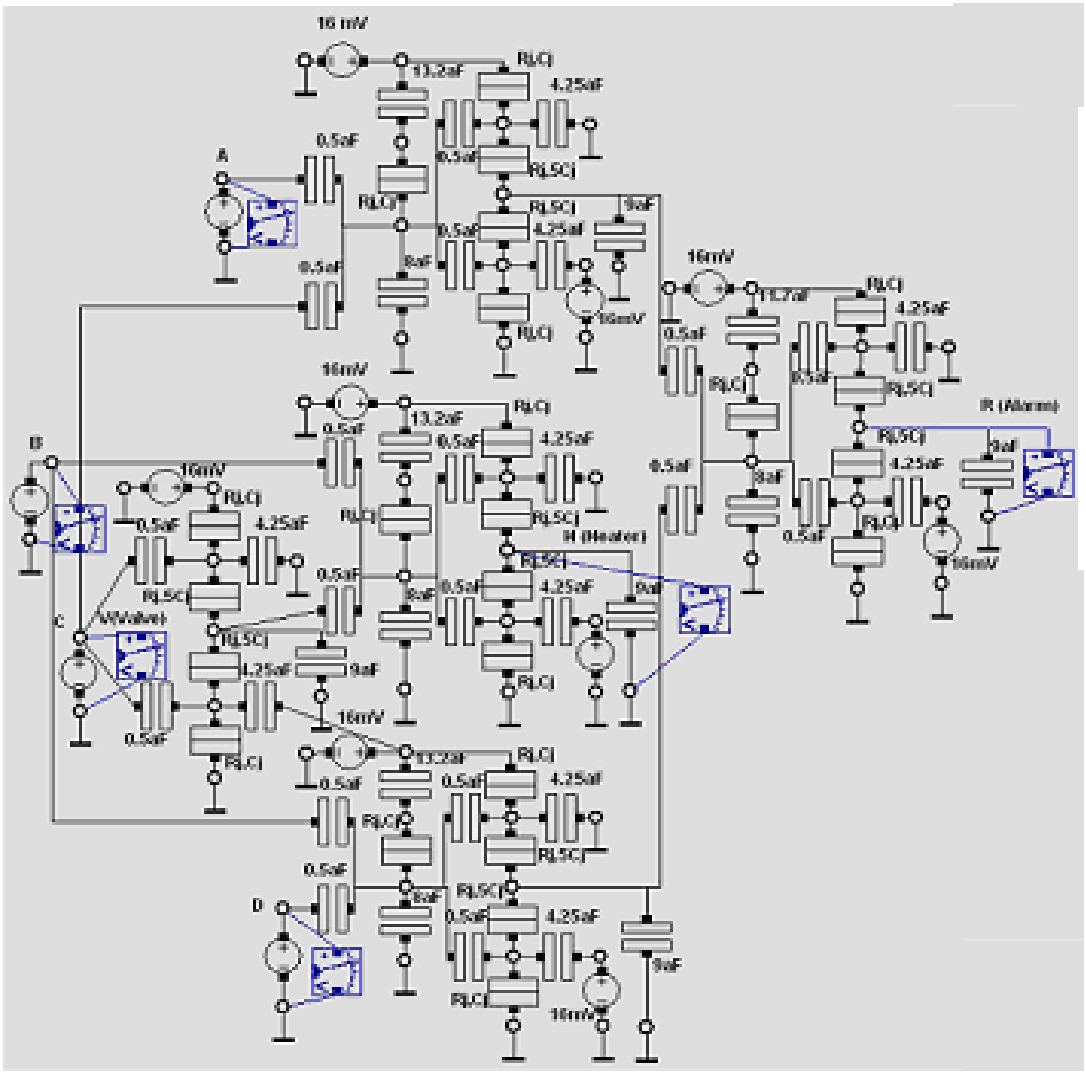
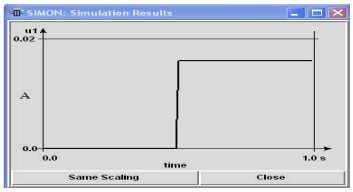
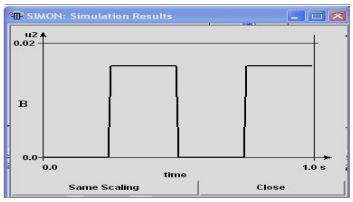


Fig. 7.Single Electron TLG based Process control circuit

Fig. 8 shows the results of the simulation. In the simulation, A, B, C and D are the input variables; H, V and R the output variables. The results obtained from the simulation are found to be satisfactory





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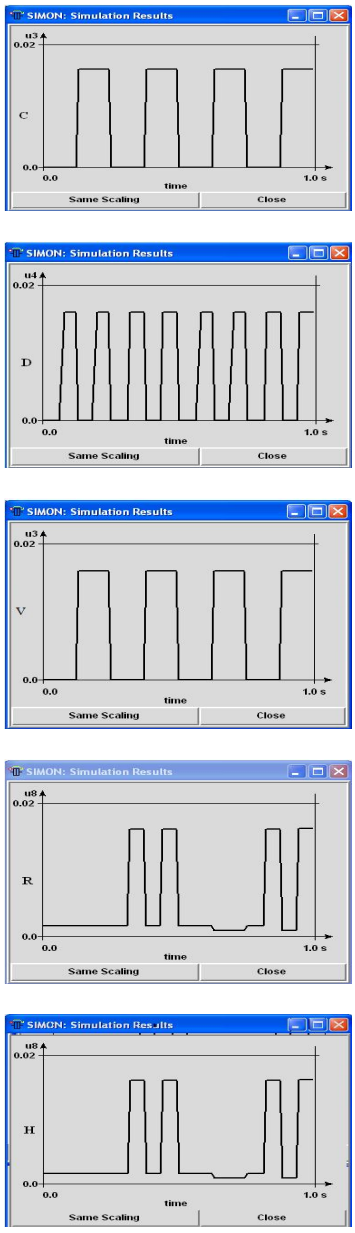

Fig. 8 Input and output waveforms

VI.CONCLUSION

The design and simulation of control unit of a process controller using Single Electron Threshold Logic Gate is presented. The complete circuit to implement the control unit has been designed and verified by simulation with SIMON. The performance of the control unit is found to be satisfactory thereby establishing the feasibility of future much faster VLSI/ULSI circuits using SET-based TLGs.

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