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Area-Delay Efficient Binary Adders in QCA

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ABSTRACT: In this paper, a novel quantum-dot cellular automata(QCA) adder design is presented that decrease the number ofQCA cells compared to previously report designs. Theproposed one-bit QCA adder design is based on a newalgorithm that requires only three majority gates and twoinverters for the QCA addition.A novel 128-bit adder designed in QCA was implemented. It achieved speed performances higher than all the existing. QCA adders, with an area requirement comparable with the cheap RCA and CFA established. The novel adder operates in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In adding together, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited. As transistors reduce in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot find much smaller than their current size. The quantum-dot cellular automata approach represents one of the possible solutions in overcome this physical limit, even though the design of logic modules in QCA is not forever straightforward.

KEYWORDS: Adders, nano-computing, QCA (quantum-dot cellular automata)

I. INTRODUCTION

In this paper, a new QCA adder design is implemented thatreduces the number of QCA cells when compared to existingreported designs. We demonstrate that it is possible to design aCLA QCA one-bit adder, with the same reduced hardware asthe bit-serial adder, as retaining the simpler clockingscheme and parallel structure of the novel CLA approach.The proposed design is based on a new algorithm thatrequires only three majority gates and two inverters for theQCA addition. It is noted that the bit-serial QCA adder uses avariant of the proposed one-bit QCA adder. By connect*n*proposed one-bit QCA adders.

A quantum-dot cellular automaton (QCA) is an attractive emerging technology suitable for the development of ultradense low-power higher-performance digital circuits. For this cause in the last few years, the design of proficient logic circuits in QCA has received a great deal of attention. Special efforts are directed to arithmetic circuits, with the major interest focused on the binary addition that is the basic operation of any digital system. Of course, the designs commonly employed in traditional CMOS designs are considered a first reference for the new design environment. Ripple-carry, carry look-ahead (CLA), and conditional sum adders were implemented in. The carry-flow adder shown in was mainly an improved RCA in which detrimental wires effects were mitigated. Parallel-prefix architectures, including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed and implemented in QCA. Recently, further efficient designs were proposed for the CLA and the BKA, and for the CLA and the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders into QCA. Theoretical formulations established for CLA and parallel-prefix adders are here exploited for the realization of a novel 2-bit addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay of just one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoiding unnecessary clock phases due to lengthy interconnections.

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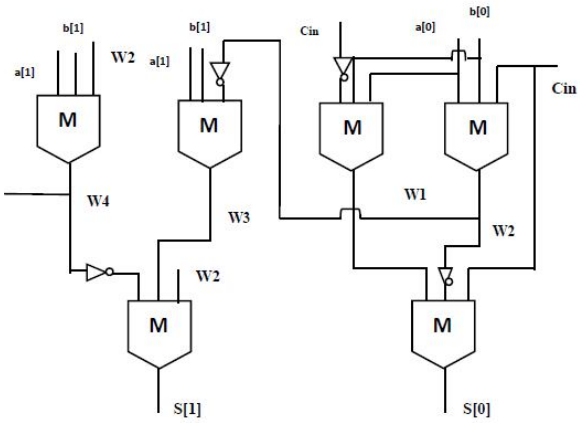

Fig 1 Novel 2-bit basic module

An adder designed as proposed runs in the RCA fashion, but it exhibit a computational delay lower than all state-ofthe-art competitors and achieves the lowest area-delay product (ADP).

II. BACK GROUND

A. QCA Basics

QCA is based on the interface of bi-stable QCA cellsconstructed from four quantum-dots. A high-level design oftwo polarized QCA cells is shown in Fig. 2. Each cell isconstructed from four quantum dots arranged in a squarepattern. The cell is charged with two electrons, which are free of chargeto tunnel between adjacent dots. These electrons tend totake up antipodal sites as a result of their mutual electrostaticrepulsion. Thus, there exist two equalenergeticallyminimal arrangements of the two electrons in the QCA cell asshown in Fig. 2. These two arrangements are denoted as cellpolarization P = +1 and P = -1 correspondingly. By using cellpolarization P = +1 to represent logic “1” and P = -1 torepresent logic “0”, binary information can be encoded.

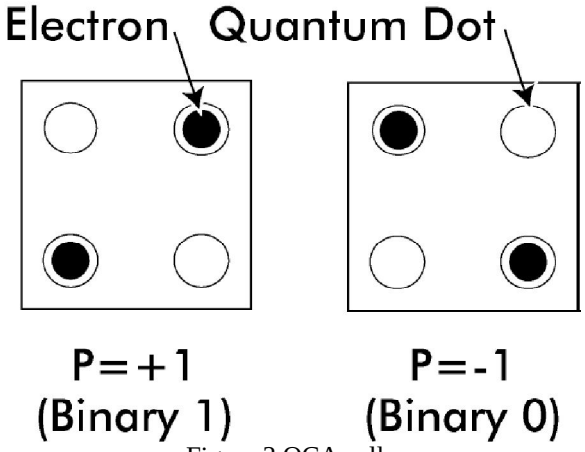

Figure 3 QCA cells

Arrays of QCA cells can be set to perform all logicfunctions. This is owed to the Columbic interactions, whichinfluences the polarization of neighboring cells. QCAdesigns have been proposed with potential barriersbetween the dots that can be controlled and used to clock QCAdesigns.

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B. QCA Logical Devices
The fundamental QCA logic devices are the QCA wire,majority gate and inverter.

QCA wire: In a QCA wire, the binary signal propagatesfrom input to output because of the Columbicconnectionsbetween cells. This is a result of the system attempting to settleto a ground state. Any cells along the wire that are anti-polarizedto the input would be at a high energy level, andwould soon settle to the correct ground state. The propagationin a 90-degree QCA wire is shown in Fig. 4. Other than the 90-degree QCA wire, a 45-dgree QCA wire can also be used. Inthis case, the propagation of the binary signal alternatesbetween the two polarizations. Advance, there exists a so-callednon-linear QCA wire, in which cells with 90-degree orientationcan be placed next to one more, but off center.

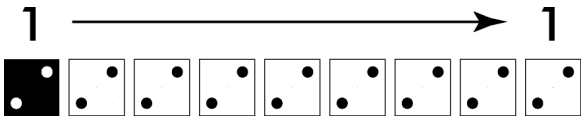

Figure 3 A QCA wire (90-degree)

Majority gate and inverter: The majority gate andinverter are shown in Fig. 4 and Fig. 5 respectively. Themajority gate performs a three-input logic function. Assumingthe inputs are A, B and C, the logic function of the majoritygate is

$$m(A, B,C) = A|B + B|C + A|C \quad (1)$$

By fixing the polarization of one input as logic “1” or “0”, wecan get an OR gate and an AND gate respectively. Morecomplex logic circuits can then be designed from OR andAND gates.

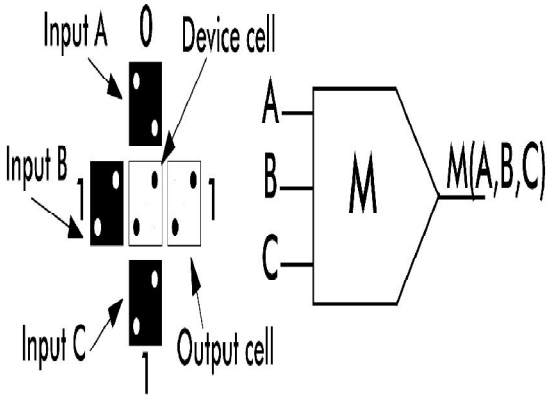

Figure 4 A QCA majority gate

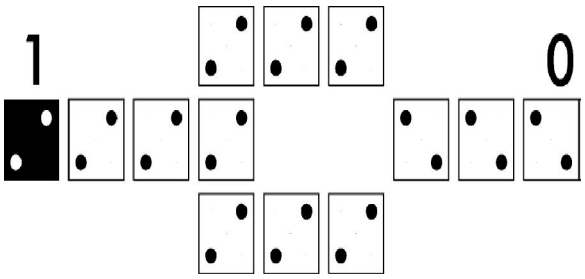

Figure5 A QCA inverter

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C. QCA Full Adders

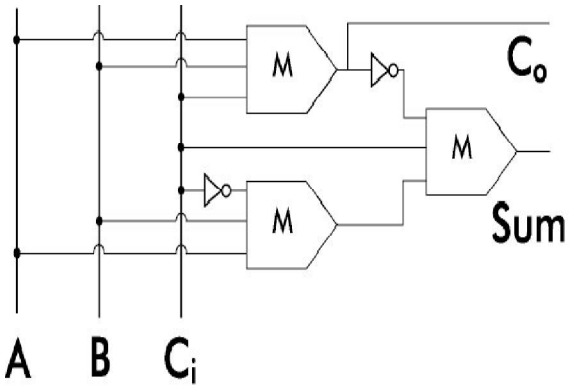

Figure 6 one-bit QCA full adder

III. PROPOSED METHOD

A QCA is a nano-structure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots inside the cell. Because of Coulombic repulsion, the two electrons will forever reside in opposite corners. The locations of the electrons in the cell determine two possible stable states that can be associated to the binary state 1 and 0.

Although adjacent cells interact through electrostatic forces and tend to arrange in a line their polarizations, QCA cells do not have intrinsic data flow directionality. To achieve controllable data directions, the cells inside a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°. This clock system named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch. QCA cells are used for both logic designs and interconnections that can exploit either the coplanar cross or bridge technique. The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs *a*, *b*, and *c*, the MG perform the logic function reported in (1) provided that all input cells are associated to the same clock signal clk*x*(with *x* ranging from 0 to 3), whereas the remaining cells of the MG are linked to the clock signal clk*x*+1

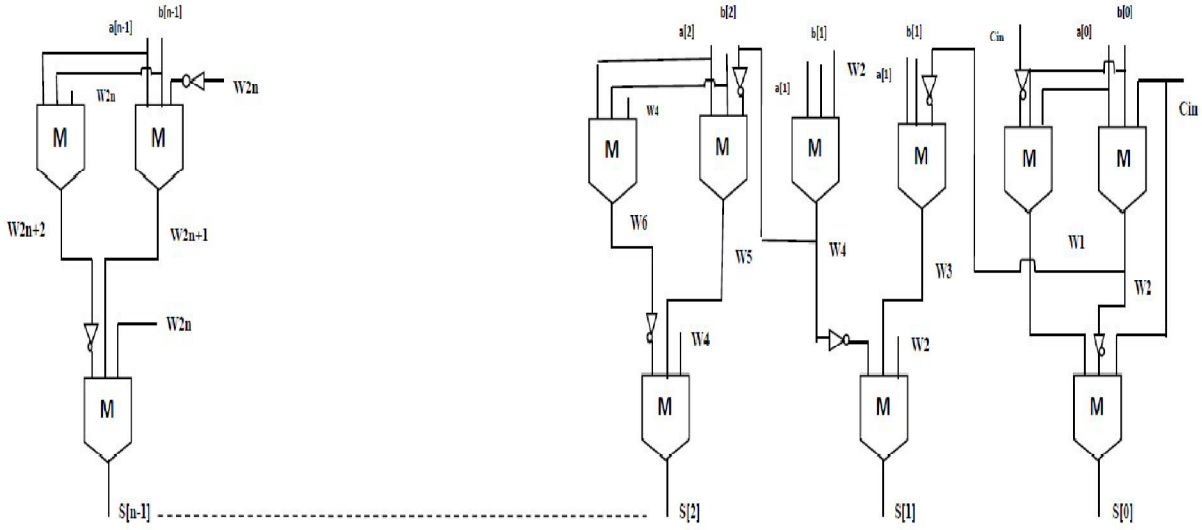

Fig 2 Novel *n*-bit adder

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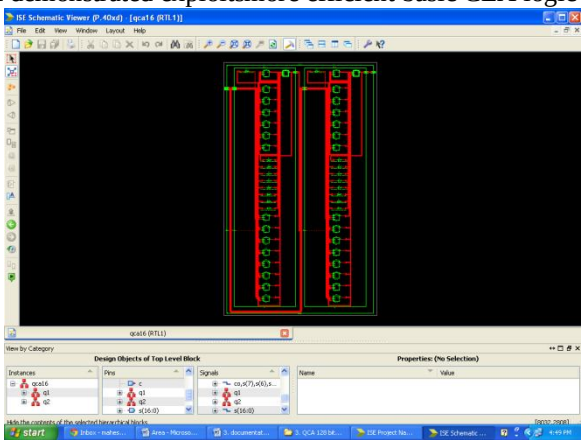
Several designs of adders in QCA exist in literature. The RCA [11], [13] and the CFA [12] process *n*-bit operands by cascading *n* full-adders (FAs). Even althoughthese addition circuits use different topologies of the genericFA, they include a carry-in to carry-out path consistingof one MG, and a carry-in to sum bit path containtwo MGs plus one inverter. As aimportance, theworst case computational paths of the *n*-bit RCA and then-bit CFA consist of (*n*+2) MGs and one inverter.A CLA design formed by 4-bit slices was also presented. In particular, the auxiliary propagate andgenerate signals, namely $p_i = a_i + b_i$ and $g_i = a_i . b_i$,are compute for each bit of the operands and then theyare grouped four by four. Such a designed *n*-bit CLA has acomputational path composed of $7+4\times(\log_4 n)$ cascade MGsand one inverter. This can be easily verified by observing that,given propagate and generate signals, to compute grouped propagate and groupedgenerate signals; four cascade MGs are introduced in thecomputational path. In addition, to calculate the carry signals,one level of the CLA logic is required for each factor of fourin the operands word-length. This means that process *n*bitaddends, $\log_4 n$levels of CLA logic are required, everycontributing to the computational path with four cascadedMGs. Finally, the calculation of sum bits introduces twofurther cascaded MGs and one inverter.The parallel-prefix BKA demonstrated exploitsmore efficient basic CLA logic designs. As its main



Novel 16-bit adder

advantage over the previously describe adders, the BKA can achieve lower computational delay. When *n*-bit operands are processed, its bad case computational path consists of $4\times\log_2 n - 3$ cascaded MGs and one inverter. Apart from the level required to compute propagate and generate signals, the prefix tree consists of $2 \times \log_2 n - 2$stages. From the logic equations provided, it can be easily verified that the first stage of the tree introduces in the computational path just one MG; the last stage of the tree contributes with only one MG; while, the intermediate stages introduce in the critical path two cascaded MGs all. Finally, for the computation of the sum bits, further two cascaded MGs and one inverter are added. With the main objective of trading off area and delay, the hybrid adder (HYBA) described combines a parallelprefix adder through the RCA. In the presence of *n*-bit operands, this architecture has a worst computational path consisting of $2 \times \log_2 n + 2$cascade MGs and one inverter.When the methodology in recent timesproposed was exploited, the worst case path of the CLA is reduced to $4 \times [\log_4 n] + 2 \times [\log_4 n] - 1$ MGs and one inverter. The above-mentioned approach can be applied also to design the BKA. In this case the overall area is reduced with respect to, but maintaining the same computational path. By applying the decomposition method demonstrated, the computational paths of the CLA and the CFA are reduced to $7 + 2 \times \log_4(n/8)$ MGs and one inverter and to $(n/2) + 3$ MGs and one inverter, respectively.

IV. NOVEL QCA ADDER

To introduce the novel design proposed for implementing ripple adders in QCA, let consider two *n*-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and suppose that for the *i* th bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $p_i = a_i + b_i$and

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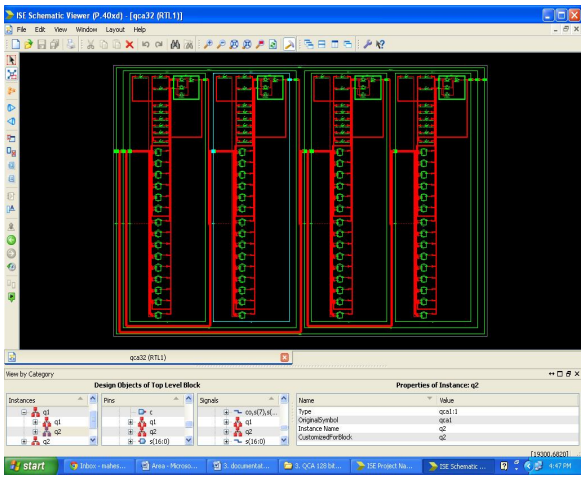
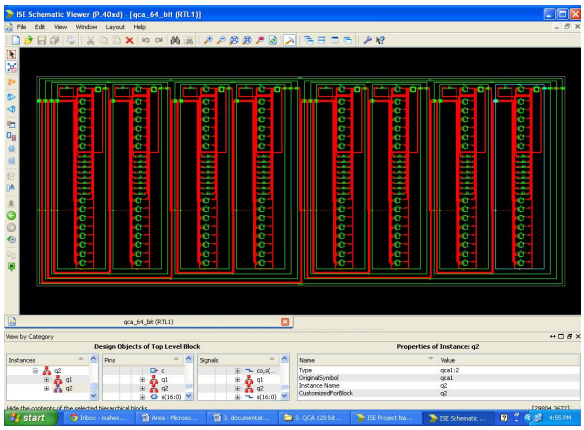


Novel 32-bit adder



Novel 64-bit adder

$g_i = a_i . b_i$, are computed$c_i$being the carry produced at the generic *(i*−1)th bit position, the carry signal *ci*+2, furnished at the (*i*+1)th bit location, can be computed using the conventional CLA logic reported. The latter can be rewritten as given in (3), by exploiting Theorems 1 and *2* demonstrated. In this way, the RCA action, needed to propagate the carry $c_i$through the two subsequent bit locations, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA. Equation (3) is exploited in the design of the novel 2-bit module shown in Figure. 1 that also shows the computation of the carry $c_{i+1} = M(p_i g_i c_i)$. The proposed *n*-bit adder is then implemented by cascading *n*/2 2-bit modules as shown in Fig. 2(a). Having assumed that the carry-in of the adder is $c_{in} = 0$, the signal p_0 is not required and the 2-bit module used at the least significant bit position is simplified.

It must be noted that the time critical addition is performed when a carry is generated at the least significant bit position and then it is propagated through the subsequent bit positions to the most significant one. In this case, the first 2-bit module computes c_2, causal to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to $(n - 2)/2$. Considering that additional two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of $(n/2) + 3$ MGs and one inverter.

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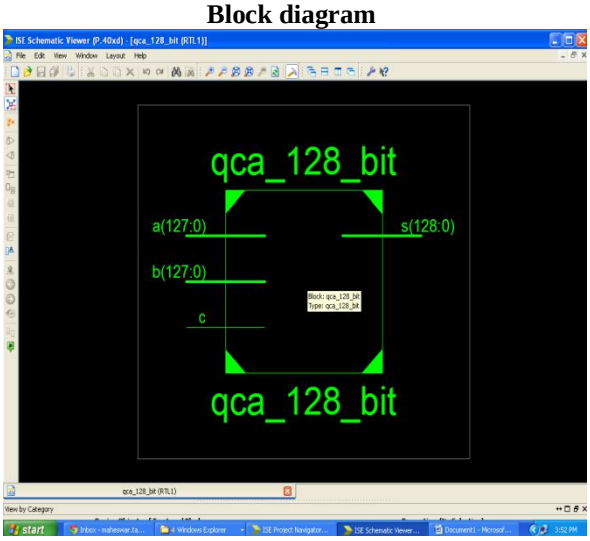
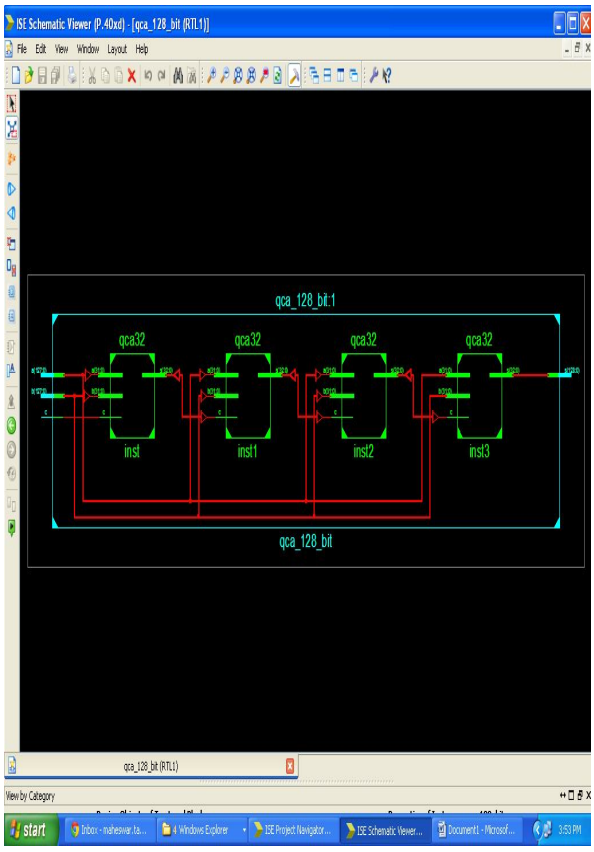
V. RESULTS

The proposed addition design is implemented for several operands word lengths using the QCA Designer tool adopting the same rules and simulation settings used.

Block diagram



RTL schematic



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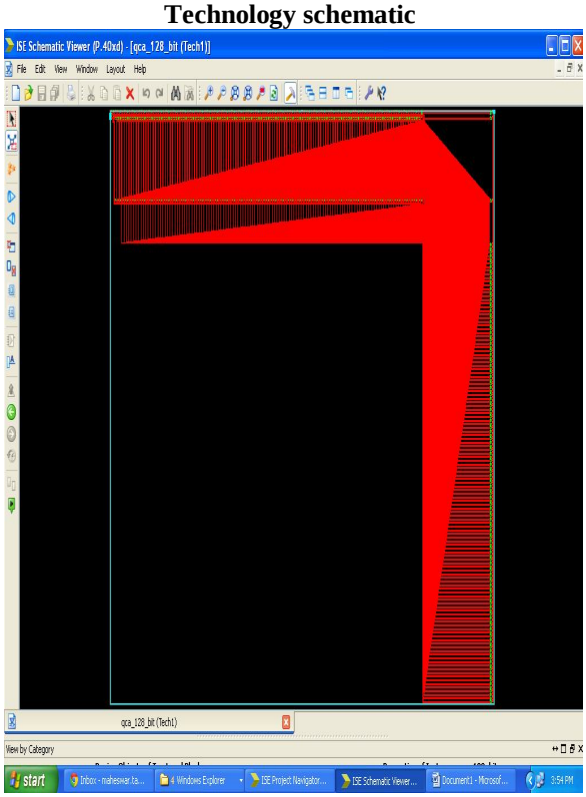
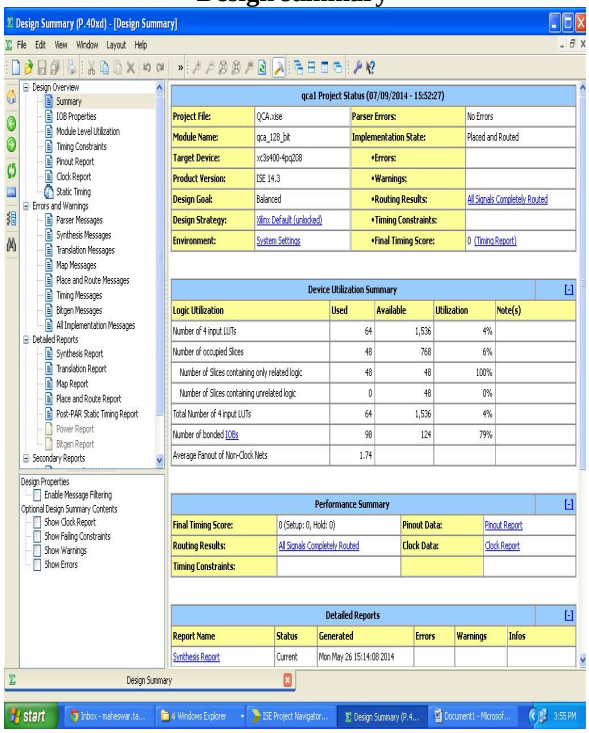
Vol. 3, Issue 11, November 2014

Technology schematic



Design summary



Simulation output

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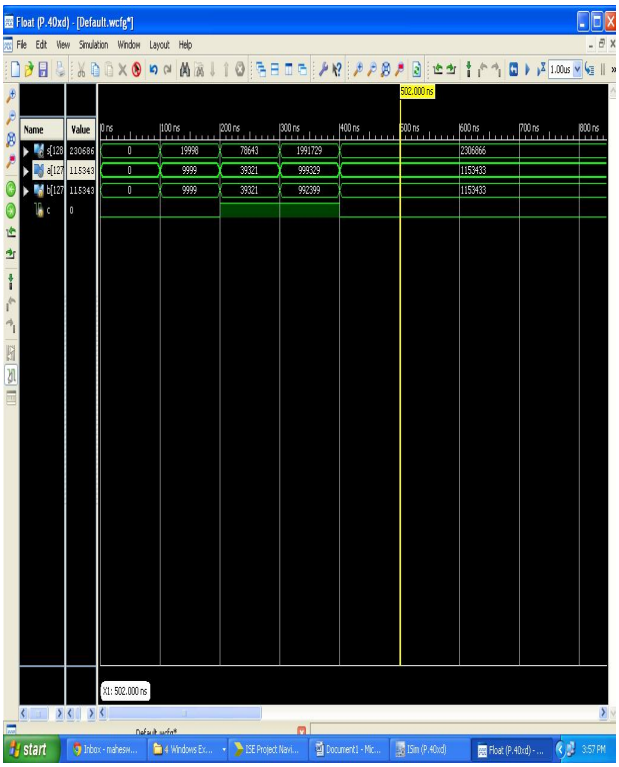

VI. CONCLUSION

A new adder designed in QCA was implemented. It achieved speed performances high than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lesser than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the explanation was limited. A 128-bit binary adder designed as described in this brief.

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