ISSN: 2319-8753

International Journal of Innovative Research in Science, Engineering and Technology
Vol. 2, Issue 6, June 2013

"Design and Development of Scalable FFT Architecture for Filter Bank De-multiplexing Application"

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Abstract: This paper proposes a high speed FFT implementation based on Radix-2^2 single path delay feedback pipelined structure which was implemented on an FPGA. The radix-2^2 algorithm is used to decrease the number of non trivial multiplication. The number of multiplication needed for calculating the FFT by this algorithm is same as that of radix-4 but its butterfly structure is equivalent to that of radix-2. The simple radix-2 structure helps in efficient VLSI implementation. The single path delay feedback structure is used for the implementation of the algorithm to make it pipelined, which is a part of the filter bank architecture for satellite application.

Keywords: *DFT,FFT,DIT,DIF,SDF,FPGA,VLSI,*

I. INTRODUCTION

The Fast Fourier Transform (FFT) is a conventional method for an accelerated computation of the Discrete Fourier Transform (DFT) [1], which has been used in many applications such as spectrum estimation, fast convolution and correlation, signal modulation, etc. Even though FFT Algorithmically improves computational efficiency, additional hardware-based accelerators are used to further accelerate the processing through parallel processing techniques. A variety of architectures have been proposed to increase the speed, reduce the power consumption, etc.

DFT Discrete Fourier Transform is the core for any digital signal process. the most efficient way to compute DFT is by FFT Fast Fourier Transform. Fourier Transform Transforms the time domain signal into frequency domain signal by which the characteristics of the signal can be analyzed. By using MATLAB we can easily find the N-point DFT of the signal, but the use of MATLAB for calculating the DFT in satellite communication (satellite) is impractical because it requires huge memory, cost and computer hardware to process. To overcome the above disadvantage a separate model is needed to be developed. Since the incoming data is unknown with respect to length, bandwidth etc, A FFT model is needed such that it can handle any amount of incoming data, such model is called as scalable FFT model. Further this scalable FFT model is used in filter banks which are used in de-multiplexing application.

II. ARCHITECTURE

TYPES:-FFT algorithms may be developed using one of three fundamental techniques

1. Number theory.

2. Matrix manipulation.

3. DFT properties [1].

As FFT is an efficient algorithm to compute the DFT.FFT uses DFT properties symmetry and periodicity properties to reduce number of complex multiplications and additions. Two approaches are used for computationally efficient algorithms for evaluating the DFT.

1. Divide and conquer approach.

2. Linear filtering operation on data.

FFT algorithms are of two types.

1. Decimation in time (DITFFT).

ISSN: 2319-8753

International Journal of Innovative Research in Science, Engineering and Technology
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2. Decimation in frequency (DIFFFT).

DIT:-In this input sequence is broken into two smaller sequences at each stage (even and odd).

DIF:-In this the input data is separated into its first N/2 and last N/2 components instead of even& odd.

The DIT/DIF may use Radix-2, Radix-4, and Radix-8 etc Butterfly structure.

The hardware architecture for scalable FFT can be divided into four classes.

1. Single PE (processing element) architecture (memory based).

a. Single memory.

b. Dual memory.

c. Triple memory.

d. Cached memory.

2. Pipe line architecture [2].

a. R2MDC(Radix-2Multipathdelay commutator).

b. R2SDF (Radix-2 Single delay feedback).

c. R4SDF (Radix-4Single delay feedback).

d.R4MDC(Radix-4Multipath delay commutator).

e.$R2^2$SDF (Radix-2^2 Single delay feedback).

3. Array based.

4. Column based.

The discrete Fourier transform X(k),k=0,1,…N-1 of the sequence x(n),n=0,1,..N-1 is defined as:

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn}$$

Where N is the transform size $W_N=e^{-j2\pi/n}$ and $j=\sqrt{-1}$.According to the decomposition method of [7] that done by substituting with

$n = (\frac{N}{2} n_1+\frac{N}{4} n_2+ n_3)_N$, $k=(k_1+2k_2+4k_3)_N$ $X(k_1+2k_2+4k_3)=\sum_{n3=0}^{\frac{N}{4}-1}[H(k_1,k_2,n_3)W_N^{n_3(k_1+2k_2)}]W_{\frac{N}{4}}^{n_3+k_3}$

Where $H(k_1,k_2,n_3)$=$[x(n_3)+(-1)^{k_1}.x(n_3+\frac{N}{2})]+(-j)^{(k_1+2k_2)}[x\left(n_3+\frac{N}{2}\right)+(-1)^{k_1}.x\left(n_3+\frac{3N}{4}\right)]$.
after this simplification, we have a set of four DFT equations of length N/4.The proposed system uses DFT properties, Divide and conquer approach[1], Decimation in frequency(DIFFFT) ,Pipe line architecture, $R2^2$SDF[3] which utilizes the delay elements more efficiently by sharing the same storage elements between the butterfly outputs and inputs. A single data stream goes through the multiplier in every stage. This architecture has the same number of butterfly units and multipliers as those in R2MDC and only N-1 delay elements, $\log_4 N$-1 Complex multipliers [1] and $\log_4 N$ butterfly units. Figure (1) shows the DIF FFT butterfly structure using the decomposition formula from 16 to 8 and then 8 to 4 and 4 to 2 point DFT. And construction of two architecture is made using the decomposition formula. These

ISSN: 2319-8753

International Journal of Innovative Research in Science, Engineering and Technology
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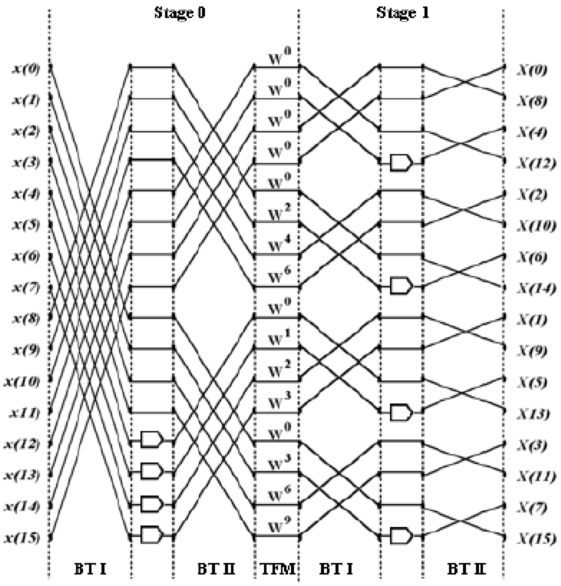
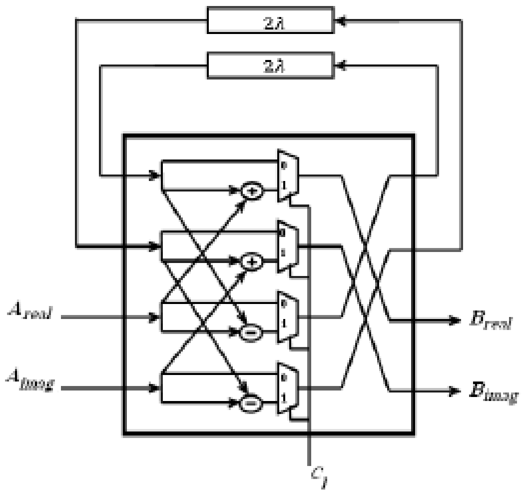
architectures are the basic building blocks for the scalable architecture.

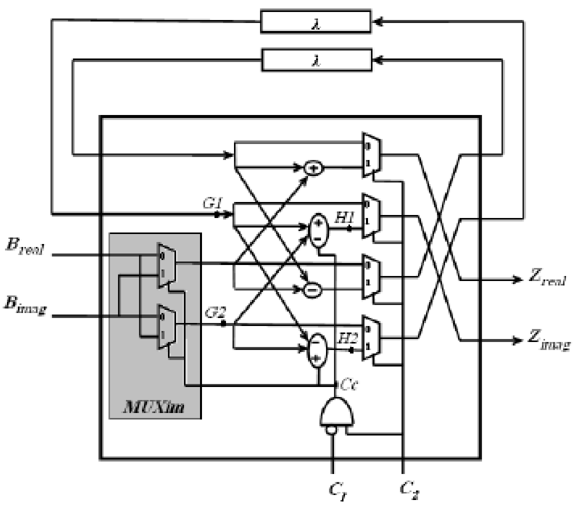




Fig(1):DIF FFT butterfly for N=16 withTWM

Fig(2)BF I structure.

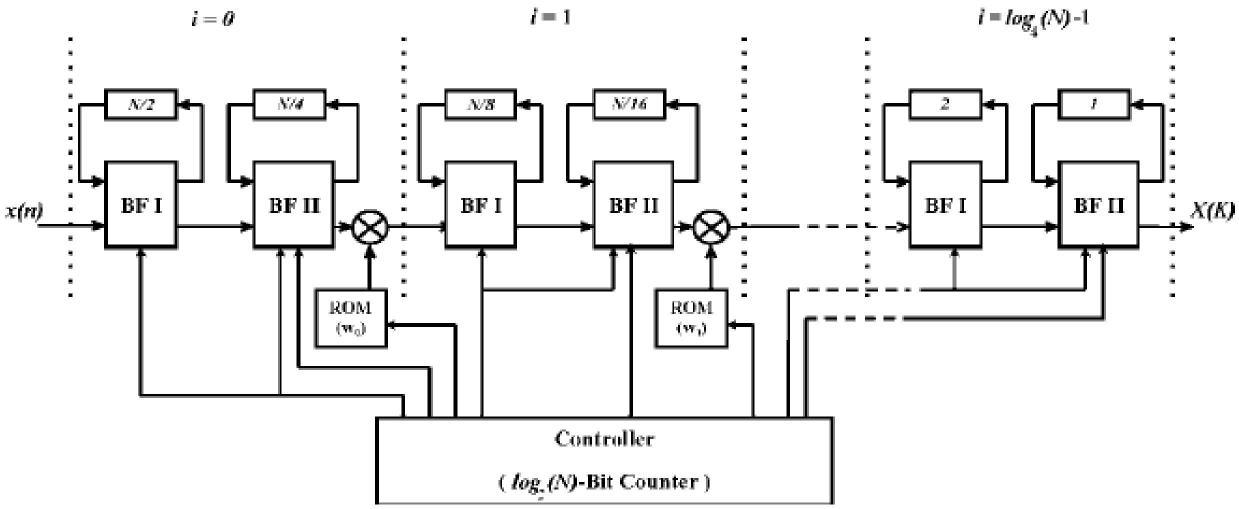
The A input comes from the previous component, TFM. The B output fed to the next component, normally BFII. In first N/2i+1cycles, multiplexors direct the



Fig(3):BF 2 Structure.

Input data to the feedback registers[6] until they are filled (position '0'). On next N/2i+1cycles, the multiplexors select the output of the adders/sub tractors (position "1"), the butterfly computes a 2-point DFT with incoming data and data stored in the feedback Registers.

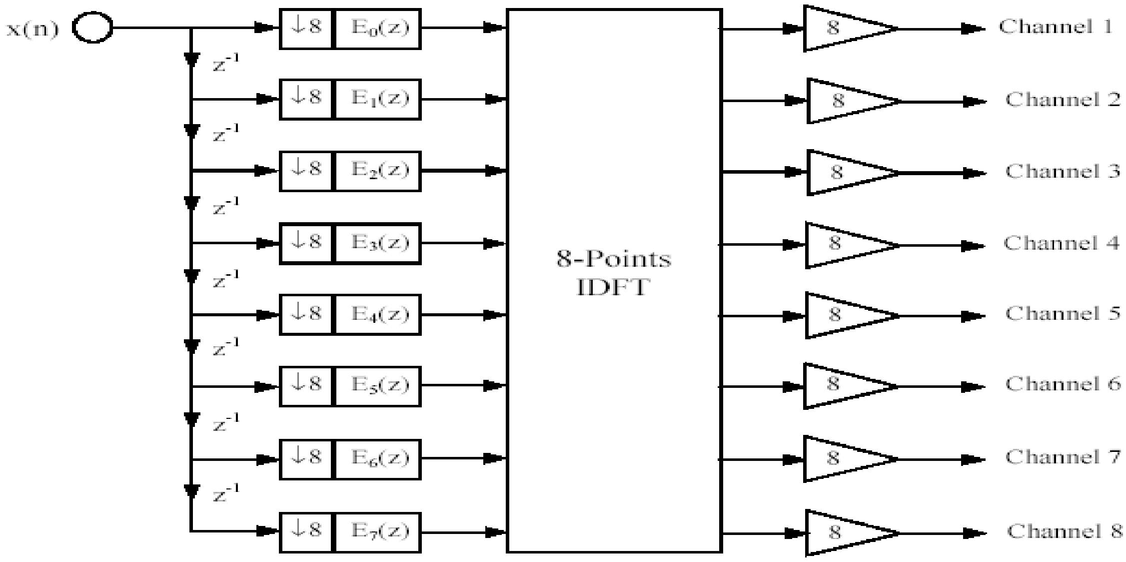
The detailed structure of BFII is shown in Fig. 3. The B input comes from the previous component, BFI. The Z output fed to the next component, normally TFM.In first N/2 i+2cycles, multiplexors direct the input data to the feedback registers until they are filled (position 0").In next N/2i+2cycles[4], the multiplexors select the output of the adders/subtractors (position 1"), the butterfly computes a 2-point DFT with incoming data and the data stored in the feedback registers.The multiplication by –j involves real-imaginary swapping and sign inversion. The real-imaginary swapping is handled by the multiplexors and the sign inversion is handled by switching the adding- delay feedback mechanism provides a solution where the first input to the butterfly is delayed until the second input is presented, after which element structure:In order to reuse the existing hardware, the delay feedback is [7]. By the time, the data appears again at the input of the butterfly. First-in First-out shift register is used to implement the delay-feedback. done by subtracting operations by mean of MUX.When the calculation can proceed. This computing on the block, it is redirected to a feedback delay line[5] by mean of multiplexers Feedback there is a need for multiplication by −j, all imaginary data are swapped and the adding-subtracting operations are switched. multiplexors switches to position "1", the real- accepting part of the data stream into the butterfly elements, but instead of used. The Control unit:Radix-2 control unit is very simple. A log(N) counter is used to switch the BF between modes. It also used as address to ROMs in order to pick the twiddle factors.



Fig(4) architecture of scalable FFT

III.FILTER BANK ARCHITECTURE

The basic block used in the demultiplexer is a digital filter bank. Starting from the frequency allocation of the incoming signal, the computational complexity of different filter bank architectures has been evaluated and the polyphase filter bank has been chosen. The basic structure of this filter bank is sketched in Fig. 5.The filter input signal (44 MSPS) is decimated by a factor 8 and enters the polyphase components Ei(z). For each component, the input rate is 5.5 MSPS. The same rate is used for the 8-points IDFT. Starting from the 4 real channels –1guard and 3 data channels- we obtain 8 complex channels, each 5.5 MHz wide. Channels number 2, 3 and 4 (useful channel) are connected to three demodulators, while the others are discarded. The Ei(z) represents the i-th polyphase component of the prototype filter,designed as low pass filter with a cutoff frequency at $\pi/8$; . Even if the FIR filter is designed with linear phase, we did not exploit its symmetry in order to reduce its hardware complexity. In fact, due to the particular structure of the polyphase filter bank, a proper sorting of the data samples is necessary and, consequently, a large amount of read/write memory should be used. For the fixed-point implementation of the polyphase component Ei(z), a filter coefficient word-length of 12 bits has been chosen starting from simulation results. The final output is obtained through an 8-points IDFT implementing the polyphase decomposition reconstruction. The channels 2, 3 and 4 carry the information corresponding to the 3 data channels. Unfortunately, the signal is complex and shifted in frequency of $\pi/2$. If additional processing is not required by the specific application, the unshifted real signal can be obtained by cascading the IDFT with a factor 2 interpolator, a half-band low-pass filter and a $\pi/2$ frequency shifter. Finally, the real part multiplied by two of the obtained signals is considered as output.



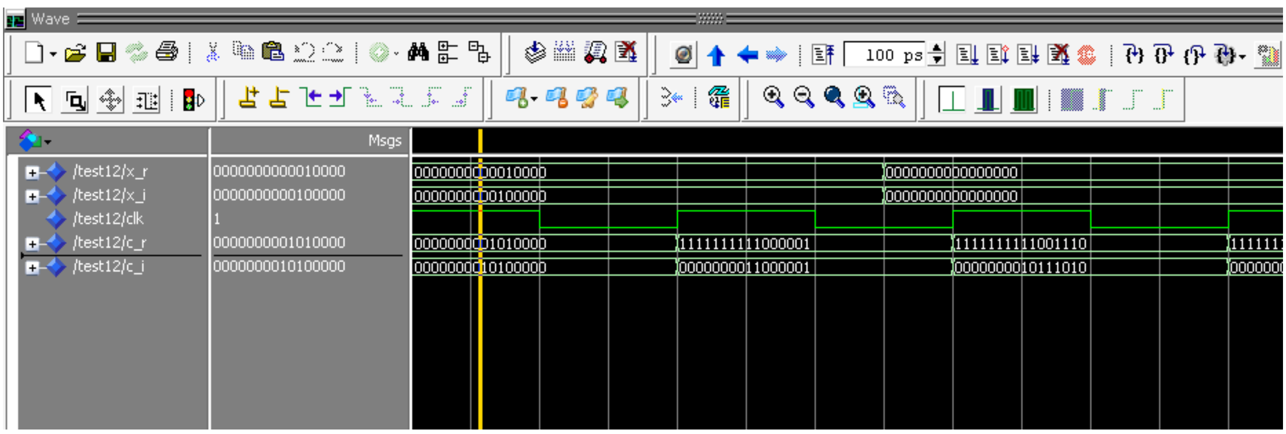
Fig(5): Filter Bank Architecture using FFT model.

IV. RESULT

The synthesized 1024-point FFT processor on VIRTEX II Pro XC2V30004FG676 can work at a maximum frequency of 43.564 MHZ dissipating 1383mW of power. Its execution speed is 26.26 µsec for calculating 1024-point FFT. The performance was measured using Xilinx Synthesis Tools, which is further used in a filter bank application in order to separate the frequency component.

V. CONCLUSION

The implemented design gives an easy way to increase the number of points of FFT as well as IFFT by imposing simple modification with the twiddle factor. The design gives the simple and efficient way for the implementation of scalable FFT. Future work includes the development of complete OFDM system and upgrade it to a multiple input multiple outputs (MIMO) system by using high density FPGA device.



Fig(6): Modelsim simulation results.
Fig(7):Design summary

ISSN: 2319-8753

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FFT_Paper Project Status (04/30/2009 - 05:47:46)			
Project File:	FFT_Paper.ise	**Current State:**	Programming File Generated
Module Name:	FFT_Saeed_Core	• **Errors:**	No Errors
Target Device:	xc5vsx35t-3ff665	• **Warnings:**	29 Warnings (7 new, 0 filtered)
Product Version:	ISE 10.1 - Foundation	• **Routing Results:**	All Signals Completely Routed
Design Goal:	Balanced	• **Timing Constraints:**	All Constraints Met
Design Strategy:	Xilinx Default (unlocked)	• **Final Timing Score:**	(Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	838	21,760	3%	
Number of Slice LUTs	1,058	21,760	4%	
Number used as logic	801	21,760	3%	
Number used as Memory	256	8,320	3%	
Number of route-thrus	7	43,520	1%	
Specific Feature Utilization				
Number of DSP48Es	44	192	22%	

ACKNOWLEDGMENT

The authors would like to thank all the anonymous reviewers for the constructive comments and useful suggestions that led to improvements in the quality, presentation, and organization of this paper. We thank Satish Sharma for his help in completing the paper and advice for the experimental implementation.

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BIOGRAPHY

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