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Design and Implementation of Reduced Area and Low Power SQRT CSLA and its Application in ALU

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ABSTRACT: In electronics, adder is a digital circuit that performs addition of numbers. To perform fast arithmetic operations, carry select adder (CSLA) is one of the fastest adders used in many data- processing processors. The structure of CSLA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate level modification is used in order to reduce the area, delay and power of CSLA. In this paper 16 –bit square root carry select adders are designed and compared. Based on the modifications, 16-bit, 32-bit and 64-bit architectures of CSLA are designed and compared. Implement conventional CSLA, BEC-based CSLA, CBL-based CSLA and Area-delay-power efficient are compared with proposed SQRT CSLA in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the existing CSLAs. Also an arithmetic logic unit is designed using the proposed CSLA. The proposed carry select adder and arithmetic logic unit is designed by using VHDL and is implemented in spartan 3E FPGA.

KEYWORDS: adder; carry select adder; square root carry select adder; arithmetic logic unit

I. INTRODUCTION

Design of area and power efficient high speed data logic systems are one of the most substantial areas of research in VLSI system design. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. In electronics applications adders are most widely used. Carry Select Adder is one of the fastest adder used in many data compressing processors to perform fast arithmetic function. To reduce the area and power consumption in carry select adder, square root CSLA architecture is used. In digital adders speed of addition is limited by the time required to propagate a carry through adder. CSLA is used to generate multiple carries and then select a carry to generate the sum. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design.

A conventional carry select adder (CSLA) consists of two ripple carry adders that generates a pair of sum and output carry bits corresponding to the input-carry (Cin = 0 and 1) and selects one out of each pair for final-sum and final-output-carry [1]. A conventional CSLA has less CPD than an RCA, but the design is not attractive since it uses dual RCA. In BEC-based CSLA, Binary to Excess-1 Converter (BEC) is used instead of RCA with Cin=1 to achieve lower area and power consumption [4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. This SQRT CSLA occupies less area, delay and low power. Further also, the parameters like delay, area and power can be reduced. By sharing Common Boolean Logic (CBL), a circuit of SQRT CSLA is proposed [6]. This proposed design is better than all the other adders in respect of area, delay and power consumption. Based on the analysis of logic operations involved in the conventional and BEC-based CSLAs, an Area-delay-power efficient SQRT CSLA is proposed [7]. This SQRT CSLA design involves significantly less area, delay and power than recently proposed CSLAs.

An arithmetic logic unit acts as the basic building blocks or cell of a central processing unit of a computer. And it is a digital circuit comprised of the basic electronics components, which is used to perform various function of arithmetic and logic and integral operations. The Arithmetic logic unit take two operands and also performs the desired operations between those units also the control signal is to be used to select the output from the operations that had been

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performed. The control unit is designed by using a multiplexer which selects the required operations. The adder unit is constructed by using proposed carry select adder. The area, delay and power efficiency of the arithmetic unit depends upon the area, delay and power of the carry select adder.

II. LITERATURE SURVEY

O. J. Bedrij in 1962 proposed an extremely fast digital adder with sum selection and multiple-radix carry [1]. He compared the amount of hardware and the logical delay for a 100-bit ripple-carry adder and a carry-select adder. The problem of carry-propagation delay was overcome by independently generating multiple-radix carries and using these carries to select between simultaneously generated sums.
Y. Kim and L.S. Kim in 2001 introduced a multiplexer based add-one circuit to reduce the area with negligible speed penalty [2]. This add-one circuit is based on a "first" zero detection logic. It generates sum of RCA2 by inverting each bit in sum of RCA1 starting from the LSB until the first zero is encountered.
Y. He, C. H. Chang, and J. Gu in 2005 proposed an area efficient square root carry select adder scheme based on a new first zero detection logic [3]. In this design, the RCAs are built with CMOS mirror topologies since this is the most interesting implementation in terms of its trade-off between power and delay performances. A new add-one circuit with less transistor count is used. The complete circuit exhibits low logic complexity and reduced power dissipation with no degradation to speed.

B. Ramkumar and H. M. Kittur in 2012 proposed the BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA [4]. The design which replaces a ripple carry block in conventional CSLA design with BEC-1 block named as Binary to Excess-1 Converter in order to reduce the area and power consumption of the regular CSLA.
I-Chyn Wey, Cheng-Chen Ho, Yi-Sheng Lin, and Chien-Chang Peng at Hong kong in 2012, proposed an area efficient carry select adder by sharing the common boolean logic term [5]. By sharing the common Boolean logic term, only need to implement one XOR gate with one INV gate to generate the summation signal pair. Also implement OR gate and AND gate to generate carry output.
S. Manju and V. Sornagopal in 2013 proposed an efficient SQRT architecture of carry select adder design by common Boolean logic [6]. The reduced number of gates of this work offers the great advantage in the reduction of area, total power and also reduces the delay.
Basant Kumar Mohanty and Sujit Kumar Patel proposed a new logic formulation for CSLA in 2014, named Area-delay-power efficient CSLA [7]. They have designed a new logic formulation for CSLA. The carry select operation is scheduled before calculation of final sum which is different from conventional approach. Due to the small carry output delay, the CSLA design is a good for the SQRT adder.

III. PROPOSED CARRY SELECT ADDER

The structure of the proposed CSLA is shown in Fig. 1. It consists of one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of CG0 and CG1 corresponding to input-carry '0' and '1'.

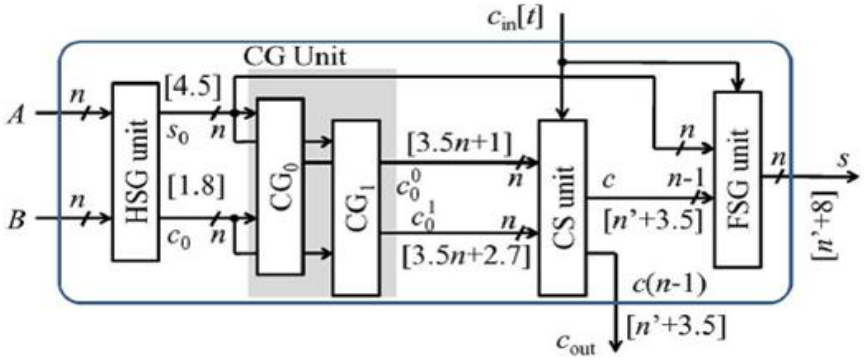

Fig. 1 Proposed Carry Select Adder

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The HSG receives two n-bit operands (A and B) and generate half-sum word S_0 and half-carry word C_0 of width n bits each. Both CG_0 and CG_1 receive S_0 and C_0 from the HSG unit and generate two n-bit full-carry words C_1^0 and C_1^1 corresponding to input-carry '0' and '1', respectively. The logic circuits of CG_0 and CG_1 units are optimized to take advantage of the fixed input-carry bits.

The CS unit selects one final carry word from the two carry words available at its input line using the control signal Cin. It selects C_1^0 when Cin = 0; otherwise, it selects C_1^1. The CS unit can be implemented using an n-bit 2-to-l MUX. However, we can find from the truth table of the CS unit that carry words C_1^0 and C_1^1 follow a specific bit pattern. If $C_1^0(i) = 1$, then $C_1^1(i) = 1$, irrespective of $S_0(i)$ and $C_0(i)$, for $0 \leq i \leq n - 1$. This feature is used for logic optimization of the CS unit. The CS unit is composed of n AND–OR gates. The final carry word c is obtained from the CS unit. The MSB of c is sent to output as Cout, and (n - 1) LSBs are XORed with (n − 1) MSBs of half-sum (S_0) in the FSG to obtain (n − 1) MSBs of final-sum (s). The LSB of S_0 is XORed with Cin to obtain the LSB of s.

A. *Reduced Area XOR Gate of Proposed CSLA:*

The proposed SQRT CSLA is designed using reduced area XOR gate, half adder, and full adder. Reduced area XOR gate has 1 gate less than the conventional XOR gate of 5 gates (AND-OR-NOT implementation) is shown in Fig.2. The main idea of proposed CSLA is to use 4 gate XOR which reduces the total gate count. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total power. In the Reduced area and low power square root carry select adder the following expression would be used for an XOR operation. Y=(A+B)(~AB).

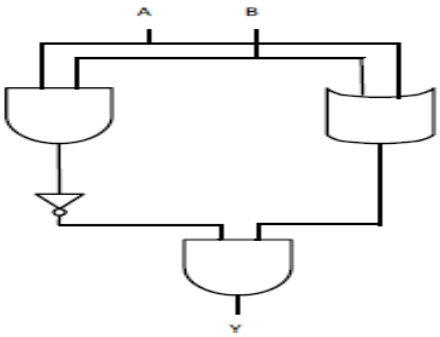

Fig. 2. Reduced Area XOR Gate

The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. The half adder using reduced XOR gate is shown in Fig. 3. Half adder using this reduced area XOR gate has 2 gates less than the conventional half adder.

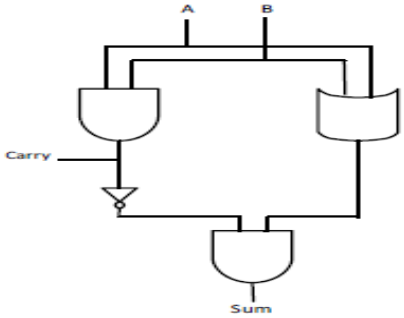

Fig. 3. Reduced Area Half Adder

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The full adder is constructed with two reduced area half adders and an AND gate shown in Fig.4 has only 9 gates, 4 gates less than conventional full adder. As the number of gates reduced in the basic building blocks of the proposed SQRT CSLA area is also reduced.

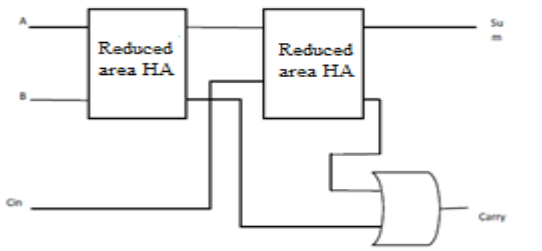

Fig. 4. Reduced Area Full Adder

IV. ALU USING PROPOSED CSLA

The purpose of this work is to propose the design of a 16-bit ALU using the proposed carry select adder and compared it with ALU using recently proposed carry select adder. The ALU designed which supports 8-bit multiplication. And the multiplier is designed using reduced area XOR gate. The functionalities of the ALU consist of following main functions like addition also subtraction, increment, decrement, AND, OR, NOT, XOR, NOR also two's complement generation. The block diagram for the proposed ALU is shown in Fig. 5.

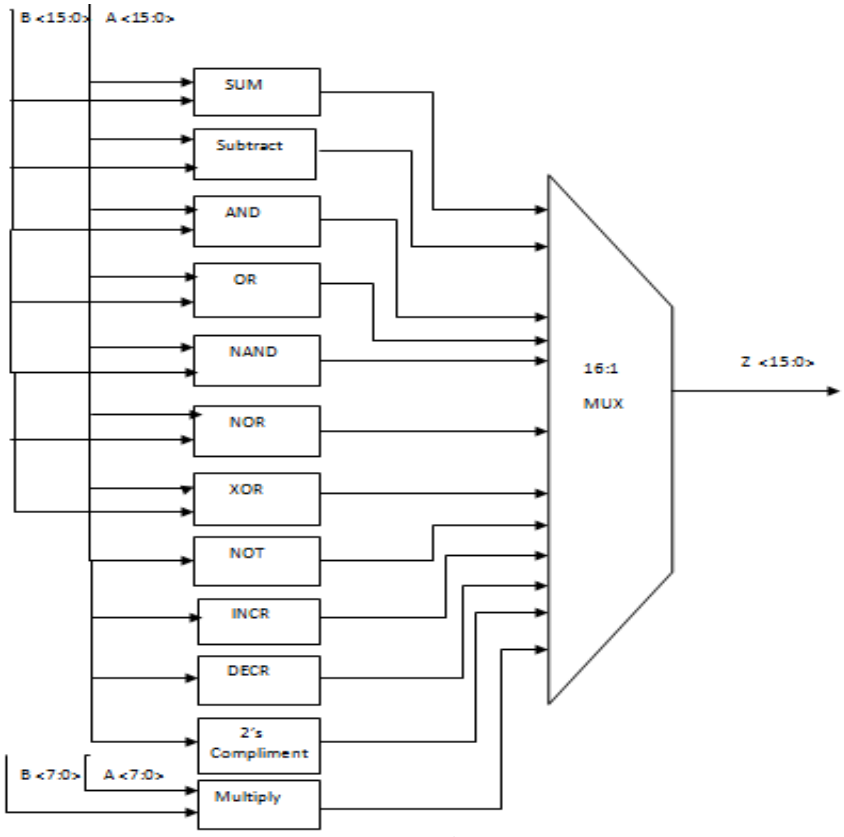

Fig. 5. Block Diagram of Proposed ALU

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In digital adders the speed of addition is limited by the time required to propagate the carry signal through the adder. In an elementary adder the generation of sum for each bit position takes place in a sequentially only after the preceding bit position has been summed and a carry is propagated into the next position. The carry select helps us in eliminating the delay caused by the propagation of the Carry signal in a binary adder. The delay caused in the addition operation is because of the carry signal. By using reduced area and low power carry select adder in arithmetic logic unit it become area and power efficient.

A 16-bit subtractor is designed for the proposed arithmetic logic unit. The 16-bit proposed ALU supports 8-bit multiplication. Multiplier is designed by using reduced area XOR gate. The incrementer and decrementer units are built using the adder and subtractor units. For increment one of the addends is given the input value logic '1'. For decrement unit the subtrahend of the subtractor is provided with logic '1' value. The two's complement generator circuit is achieved by using an inverter and an incrementer. The input operand is passed through an inverter which inverts its digits. The output of the inverter is given as input to the incrementer. The incrementer adds logic 1 to the inverted bits. Thus the output generated is the two's complement of the input bit.

The multiplexer is used to select the desired output. All operations are performed in a single cycle but only the required operation is selected by the multiplexer. Table 1 shows the operations and their opcodes of the proposed arithmetic logic unit.

Table 1. Operations and their Opcodes

Operation	Opcode	Operation	Opcode
SUM	0001	NOR	0111
Multiply	0010	XOR	1000
Subtract	0011	Increment	1001
AND	0100	Decrement	1010
OR	0101	NOT	1011
NAND	0110	Two's Compliment	1100

V. SIMULATION AND IMPLEMENTATION RESULTS

The proposed design is developed using VHDL and synthesized using XILINX 13.2 and is simulated in ISim for Spartan-3E FPGA series. Simulation result of 16-bit proposed carry select adder is shown in Fig. 6.

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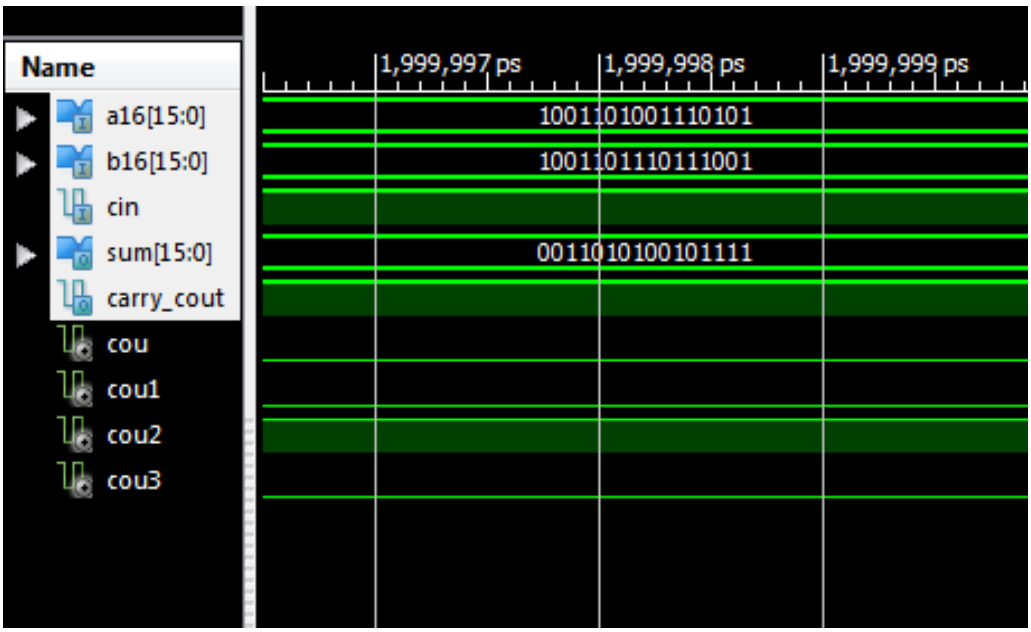

Fig. 6. Simulation Result of 16-bit Proposed CSLA

The comparison of area, delay and power consumption for the 16-bit conventional CSLA, BEC-based CSLA, CBL-based CSLA, Area-delay-power efficient CSLA and proposed CSLA designs is shown in Table 2. The number of gates used in the design indicates the area of design. The power consumption is measured in terms of total power and dynamic power. The numbers of gates used in the design of proposed CSLA are fewer than the existing CSLAs. The reduced number of gates of the proposed CSLA offers a great advantage in the reduction of area and total power consumption. Also the proposed carry select adder has less delay than existing CSLAs.

Table 2. Comparison of Area, Delay and Power Consumption of CSLAs

Design	Bits	Area (No.of Slices)	Delay (ns)	Total Power (mw)
Conventional CSLA	16	30	15.58	248
BEC-based CSLA	16	26	13.753	240
CBL-based CSLA	16	24	22.603	234
Area-delay-power efficient CSLA	16	20	10.192	229
Proposed CSLA	16	18	9.894	221

A 32-bit proposed carry select adder is designed and compared its area, delay and power consumption with recently proposed carry select adder. The simulation result of 32-bit proposed CSLA is shown in Fig. 7.

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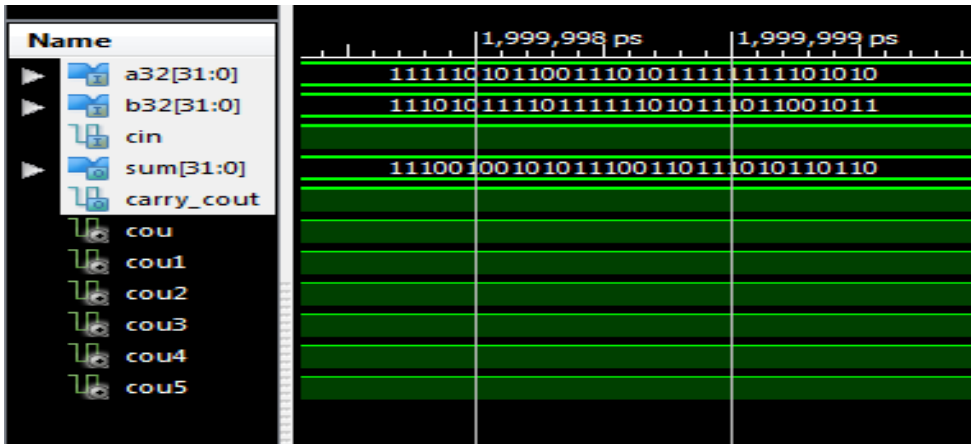

Fig. 7. Simulation Result of 32-bit Proposed CSLA

A 64-bit proposed carry select adder is designed and compared its area, delay and power consumption with recently proposed carry select adder. The simulation result of 64-bit proposed CSLA is shown in Fig. 8.

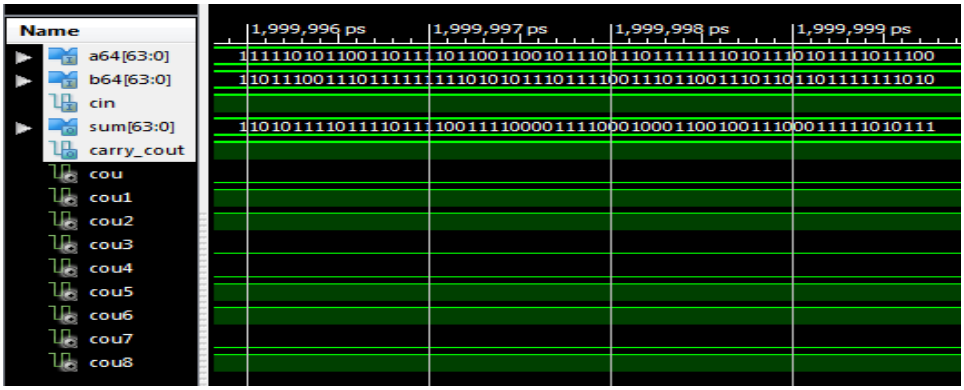

Fig. 8. Simulation Result of 64-bit Proposed CSLA

The comparison of area and power for the 16-bit, 32-bit and 64-bit Area-delay-power efficient CSLA (recently proposed design) and proposed CSLA designs is shown in Table 3. It is clear that area and power of proposed SQRT CSLA for 16-bit, 32-bit and 64-bit is reduced as compared recently proposed carry select adder.

Table 3. Comparison of Area, Delay and Power Consumption of Different Width CSLAs

Design	Width (n)	Area(No .of Slices)	Total Power (mw)
Area-Delay-Power Efficient CSLA	16	20	229
	32	57	374
	64	113	579
Proposed CSLA	16	18	221
	32	48	357
	64	101	553

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A 16-bit ALU using proposed CSLA is designed. Simulation result of 16-bit ALU using proposed carry select adders is shown in Fig. 9.

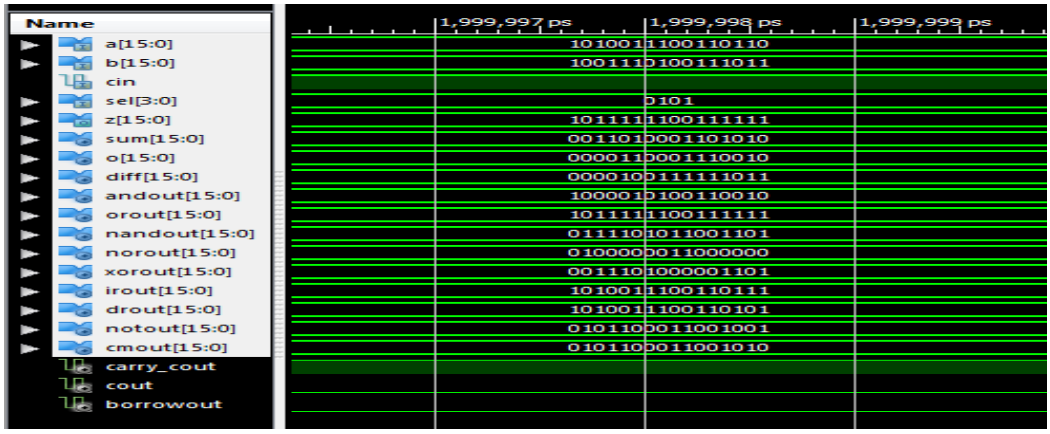

Fig. 9. Simulation Result of ALU Using Proposed CSLA

The comparison of area and power for the 16-bit ALU using Area-delay-power efficient CSLA (recently proposed design) and ALU using proposed CSLA design is shown in Table 4. It is clear that area and power of ALU using proposed SQRT CSLA is reduced as compared to ALU using recently proposed CSLA.

Table 4. Comparison of Area and Power Consumption of ALUs

Design	Bits	Area (No.of Slices)	Total Power (mw)
ALU using Area-Delay-Power Efficient CSLA	16	237	116
ALU using Proposed CSLA	16	212	104

VI. CONCLUSION

Power, delay and area are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The proposed SQRT CSLA has low power, less delay and reduced area than existing SQRT CSLAs. Also the proposed CSLA is little bit faster than existing CSLAs. The ALU designed using proposed CSLA has reduced area and power than ALU using recently proposed CSLA. Less area and faster operation makes the ALU ideal for an efficient logic circuit.

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BIOGRAPHY

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