ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

Design of Network on Chip with an Arbiter

Gopika Santhosh

M. Tech Scholar (VLSI & Embedded Systems), Dept. of ECE, IIET, MG University, Kottayam, Kerala, India.

ABSTRACT: Network on Chip (NoC) is one of the solutions for faster on chip communication, possible through routers. This paper presents an NOC with a router containing loopback module, error journal and an arbiter to reduce data loss and congestion. The presented mechanism can distinguish between permanent and transient faults. It can localize and isolate faulty parts in routers of NOC such as bus, input port and output port. This paper is mainly focused on the router design, routing algorithm, and arbitration algorithm and buffer mechanism.

KEYWORDS: Network on Chip, Arbiter, routing algorithm

I. INTRODUCTION

A rapid progress in Very Large Scale Integration (VLSI) in the past recent years has resulted in the fabrication of millions of transistors on a single silicon chip. With the current CMOS technology it is possible to implement a design with approximately one billion transistors on a single chip. This advancement in the micro-electronics leads to the integration of various components of a computing system or any other electronic system on a single Integrated Circuit (IC) to implement a complete system on a chip (SoC). Now, the trend has moved to more complex multiprocessor systems-on-chip (MPSoC) [1] to meet the current requirements of real time systems.

Network on Chip (NoC) comprises of routers and interconnections and relies on data packet exchange for the sake of communication between PEs and IPs.The data is transferred between the source and destination with the help of a routing algorithm. Routing methods can be classified into two types, namely, source routing and distributed routing. In distributed routing, the header contains destination address only and the path is computed dynamically by participation of routers on the path. A very large number of routing algorithms have been proposed in literature. Since the paths in source routing are pre-computed offline, therefore source routing can provide no or limited path adaptivity in the case of faults and traffic congestion. A modified XY routing [2] is used throughout this paper.

Topology [3] is a very important feature in the design of NoC because design of a router depends upon it. Commonly used topologies are mesh, ring, torus, binary tree, bus etc. Some researchers have also proposed topologies suitable for an application or an application area. Mesh topology will be used throughout in this paper.2-D mesh topology is suitable for field programmable gate array systems (FPGA).

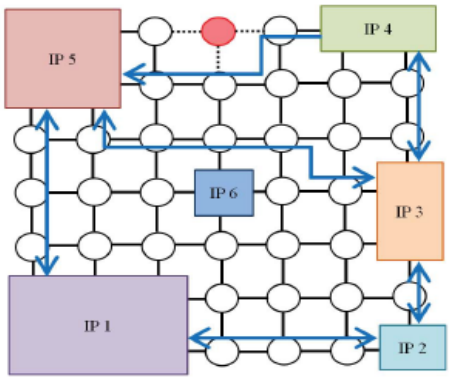

Fig. 1. Bypassing in NoC

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

MPSoCs are sensitive to phenomena that generate permanent, transient, or intermittent faults [4]. These faults may lead to data packet losses or permanent routing errors [5]. Specific error detection blocks have to be used in the network to detect the errors and locate the faulty sources. Also, permanent errors have to be distinguished from transient errors and exact location of permanent faulty parts of the NoC must be determined, to bypass them using the adaptive routing algorithm. Along with this, error correcting codes (ECCs) are to be implemented inside the NoC components. Of the different techniques, the end-to-end [6], the switch-to-switch detection and code-disjoint approach [6] are mainly used. These mechanisms cannot isolate just the faulty parts of the NoC and cannot differentiate permanent and transient faults, hence are not accurate. In addition, adds cost in terms of logic area, latency in data packet transmission, and power consumption. The adaptive XY algorithm [1] is livelock-free and deadlock-free and allows bypassing the faulty regions. The adaptive XY algorithm relies on comparison of source and destination address and determination of the XY path.

This paper presents a reliable dynamic NOC (fig. 1) with a mesh structure of routers which is able to bypass faulty locations with the help of modified XY routing. It can also detect and correct the data packet errors to an extent, thus avoid data corruption. It also uses self loopback mechanism avoiding data loss, localizing permanent sources of errors while maintaining the performance of NOC.

II. PROPOSED ARCHITECTURE

The proposed architecture of the rkt-switch is shown in fig. 2. It is suitable for a 2-d mesh NoC, having four directions (north, south, east, and west) and the PEs and IPs can be connected directly to any side of a router. So, there is no specific connection port for a PE or IP. The proposed architecture comprises a no of blocks like, loopback module [2], ECC, routing error detection, routing logic, i/o ports, input buffers, arbiter, error journal and control signals. The operation is based on store and forward technique in which, at each node the packets are stored in buffer and directed according to routing algorithm and the technique is referred to as store-and-forward (SAF) [7].

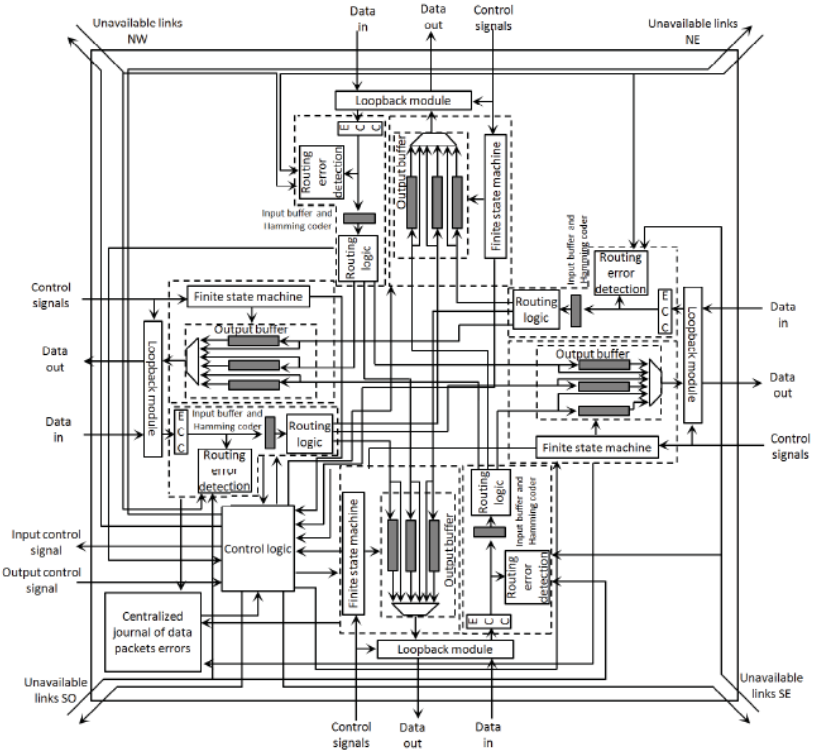

Fig. 2. Architecture of rkt-switch

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

The rkt-NoC uses non bouncing routers, if the router is surrounded by three unavailable neighbour routers, then it also become unavailable. The data flow is controlled using hand shaking signals like ack/nack solutions, as usual relies on retransmission of data packets. The Hamming ECC is apt for rkt-switch, as it permits the correction of single event upset (SEU) errors and detection of multiple event upset (MEU) errors. The distinction between permanent and transient errors is made possible by an error journal which saves data transmission results and self-loopback mechanism.

A. *XY Routing:*

Routing is the important point to be considered, for the faster and reliable on-chip communication. There are different routing algorithms available in [7], [8], [9], [10]. Routers are addressed in the matrix format. Modified XY-routing is a simple deterministic routing algorithm, where messages are transmitted completely as a packet. In a 2-D mesh network, XY-routing first routes packets along the X-axis. Once it reaches the destination's column, the packet is then routed along the Y-axis until the destination router is reached. If any particular router is unavailable it is checked with the help of an error journal and thus bypassed hence called modified XY algorithm. This bypassing decision is then verified with the help of DAI links. If three consecutive errors occurs while data transmission then it is considered as a permanent error and is noted in the error journal and the particular error source is isolated in the NoC router. When the router receives the packet it decodes the code for error checking and corrected accordingly and then routing logic is applied. Next, the results are passed to an arbiter who directs the data to the corresponding output line after encoding it.

B. *Loopback Module:*

The RKT switch consists of a loopback module which is used to make a new path for the packets by looping back through another port. It is done if and only if the current router found any fault in the neighbour router to which the packet has to be sent. Router checks the availability of the neighbouring router, if it is available the packet is sent and no loopback required but if neighbour is unavailable the data is loop backed. The circuit representation of this loopback module is given in Fig.3 which consists of buffers, multiplexer, a cross bar switch and control logic to control the operation.

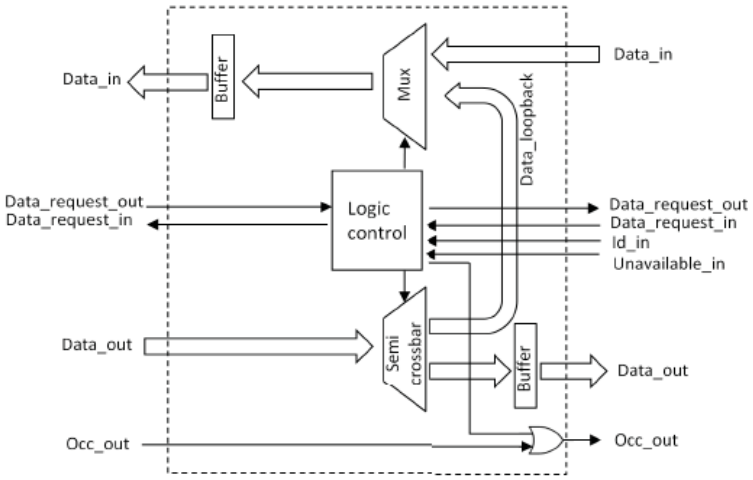

Fig. 3. Architecture of loopback module

In the operation of loopback module it initially checks the data request in signal from the router to which it has to send the packet if it is high and the unavailability link is low then the control logic generates control signal for multiplexer and the crossbar switch to pass the message in and out through the loopback module and activates the data request out signal. Similar to this function there were another two condition that is the data request in signal is low and the availability link is either low or high or else the availability link is low and the data request in signal is high, the

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

control logic generates the control signal for multiplexer and the crossbar switch to loopback the signal through another port.

C. *Arbiter:*

Arbiter controls the arbitration [7] of the ports and resolves contention problem. It keeps the updated status of all the ports and knows which ports are free and which ports are communicating with each other. The role of arbiter is shown in the fig. 4 with necessary inputs and outputs. Packets of different input ports may have to go to the same output. This selection is made by the arbiter, which decides in which order the packets will be served and to which ports. The inputs of the arbiter will be the requests from neighboring routers (north, south, east, and west) and the outputs of routing logic. Based on the priority we set and analyzing the inputs we can direct the data to the port and can reduce data congestion and data loss. Arbitration works only when there is more than one request for the same port otherwise data flow occurs normally. The role of arbiter is shown in the fig. 4 with necessary inputs and outputs.

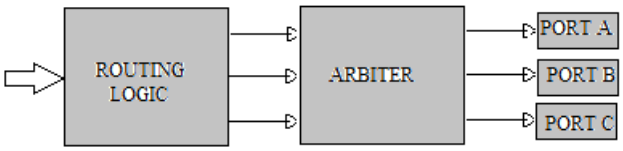

Fig. 4. Arbitration of ports

III. PROPOSED ALGORITHM

A. *Modified XY Routing:*

- Address of routers is specified in matrix format and data has to be routed from source to destination.
- Let the current router address be (Cx, Cy) and destination address be (Dx, Dy).
- First, data is directed along X direction, comparing Cx and Dx till Cx equals Dx.
- Once the address of source and destination router become same along the X direction, then Dy and Cy are compared till they become equal.
- From address comparisons the router checks the previous routing decision obeyed routing logic with the help of DAI links (NW, NE, SE, and SW) along the four diagonal directions.
- If the previous XY path is unavailable then the previous routing decision was a correct bypass otherwise it is a routing error.
- The latter is considered as a permanent error for the corresponding block in the error journal.
- If any port is unavailable then new path is established to bypass the faulty port and thus, avoid data loss.

IV. SIMULATION RESULTS

The proposed design is developed using VHDL and synthesized using XILINX 13.2 and is simulated in ISim for Spartan-3E FPGA series. A 2×3 mesh network is simulated and 1×3 mesh network is implemented in Spartan-3E FPGA series. 1×3 mesh network will have three rkt switches arranged in a line. The data size used is 31 bit and so the decoded output is 25 bit. All the blocks share a common clock source. Bypassing is shown by making a particular port erroneous. The main advantage of the proposed system is that only the faulty port is disconnected and the loopback mechanism ensures that data is never lost. The simulation results are shown below:

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

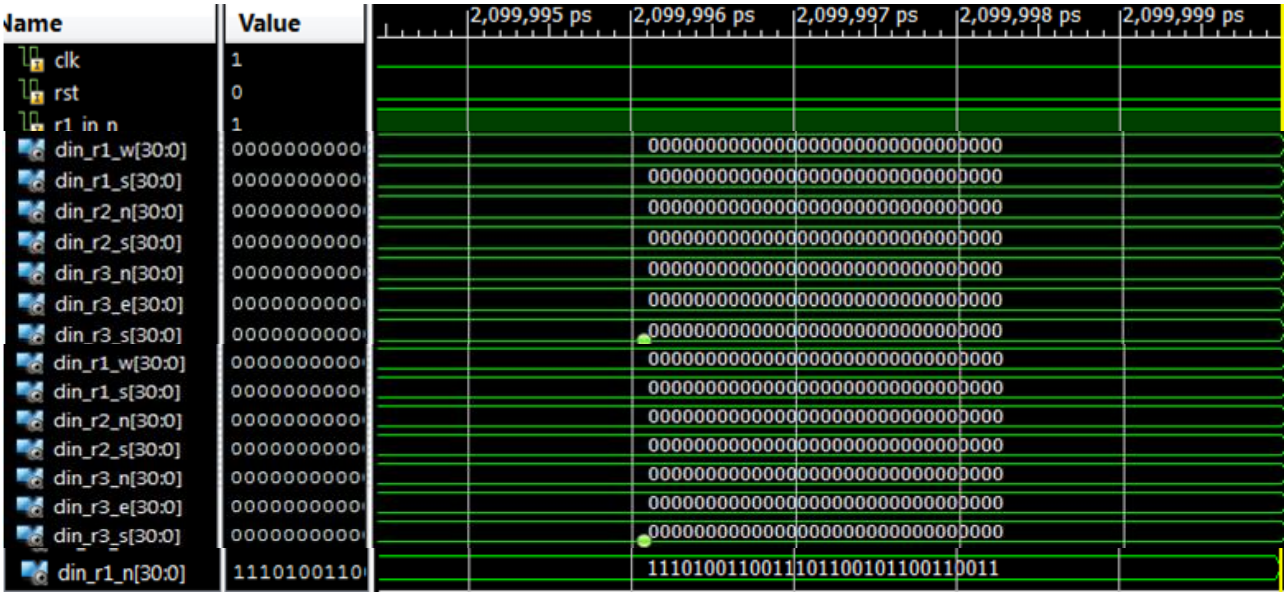

Fig. 5. Inputs of 1×3 mesh using rkt switch

Fig.5 shows the different inputs given to 1×3 NoC. In the result, din represents the 31 bit input data given to router. Here data "11101001100111011001011001100 11" is given as input to the north input of router r1 and r1_in is the request for the same. All other data inputs are set as "00000000000000000000000000000000".

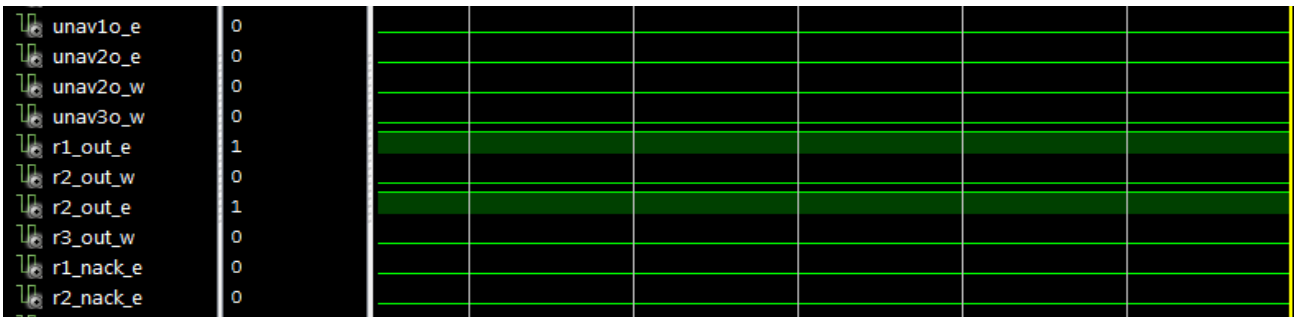

Fig. 6. Data flow in 1×3 mesh using rkt switch

Fig.6 shows the flow of data by setting r1_out_e and r2_out_w as '1'. This r2_out_w will be the request input for router r3. Fig.7 indicates the address of the three routers in matrix format as "0000", "0100" and "1000" and final output.

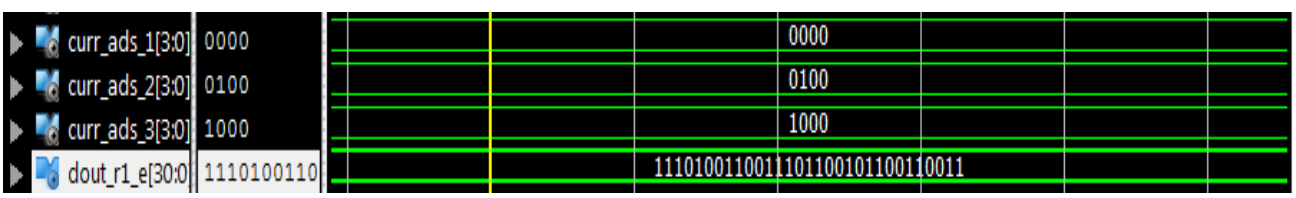

Fig. 7. Output of 1×3 mesh using rkt switch

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

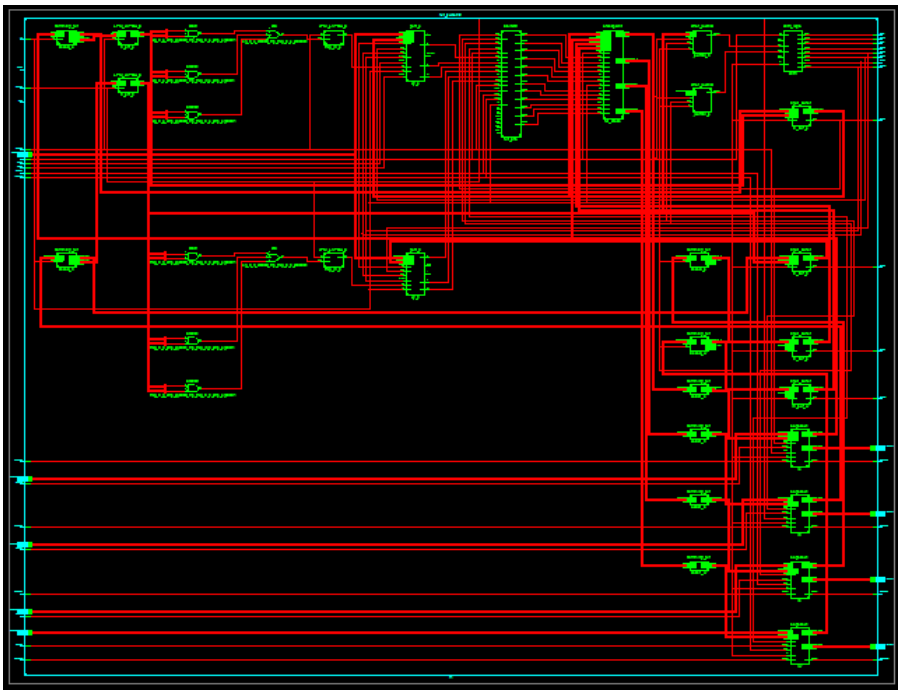

Fig. 8. RTL view of 1×3 mesh using rkt switch

Fig. 8 shows the RTL view of the 1×3 mesh network with three rkt-switches each with loopback module, arbiter, buffers, decoder and encoder, error journal and control logic.

V. CONCLUSION

The RKT-NoC is highly reliable when compared with ordinary NoC due to the addition of error detection mechanism in the design and it avoids the dead lock and live lock problem. Routing algorithm based on XY logic allows the bypassing of unavailable components. The presented technique can also distinguish between permanent and transient errors and localize error sources more accurately than switch-to-switch and code-disjoint techniques. It also has the advantage of disconnecting only the faulty part like bus, input port or output port. Further the use of loopback module and arbiter serves the data from loss.

REFERENCES

1. K. Sekar, K. Lahiri, A. Raghunathan, and S. Dey, "Dynamically configurable bus topologies for high-performance on-chip communication,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 16, no. 10, pp. 1413–1426, Oct. 2008.
2. Cédric Killian, Camel Tanougast, Fabrice Monteiro, and Abbas Dandache,' Smart Reliable Network-on-Chip', IEEE transactions on Very Large Scale Integration (VLSI) systems, vol. 22, no. 2, February 2014
3. Saad Mubeen,'Evaluation Of Source Routing For Mesh Topology Network On Chip', Jonkoping Institute of Technology.
4. C. Grecu, L. Anghel, P. Pande, A. Ivanov, and R. Saleh, 'Essential fault tolerance metrics for NoC infrastructures,' in Proc. Int. On-Line Test.Symp., 2007, pp. 37–42.
5. P. Frantz, L. Carro, E. Cota, and F. L. Kastensmidt, "Evaluating SEU and crosstalk effects in network-on-chip routers," in Proc. 12th IEEE Int. Symp. On-Line Test., Jul. 2006, pp. 191–192.
6. C. Grecu, A. Ivanov, R. Saleh, E. Sogomonyan, and P. Pande, "On-line fault detection and location for NoC interconnects," in Proc. 12th IEEE Int. On-Line Test. Symp., Jul. 2006, pp. 145–150.
7. Anurag Shrivastava, Amit Kant Pandit,' Design and Performance Evaluation of a NOC- Based Router Architecture for MPSoC ', 2012 Fourth International Conference on Computational Intelligence and Communication Networks.
8. J. Wu, "A fault-tolerant and deadlock-free routing protocol in 2d meshes based on odd-even turn model," IEEE Trans. Comput., vol. 52, no. 9, pp. 1154–1169, Sep. 2003.
9. W. Dally and C. Seitz, "Deadlock-free message routing in multiprocessor interconnection networks," IEEE Trans. Comput., vol. C-36, no. 5, pp. 547–553, May 1987.

ISSN(Online): 2320-9801
ISSN (Print): 2320-9798

International Journal of Innovative Research in Computer and Communication Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 9, September 2015

10. M. Majer, C. Bobda, A. Ahmadinia, and J. Teich, "Packet routing in dynamically changing networks on chip," in Proc. 19th IEEE Int.
11. Parallel Distrib. Process. Symp., Apr. 2005, p. 154b.

BIOGRAPHY

Gopika Santhosh is an M Tech scholar in VLSI and Embedded Systems in the Electronics and Communication Department, IIET, MG University. She received B Tech degree in 2013 from M.G. University, Kottayam, Kerala. Her research interests are VLSI and HDL languages etc.