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FPGA Implementation of High Speed Linear Convolution Using Vedic Mathematics

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ABSTRACT:-Convolution is a mathematical operation, just as multiplication, addition. It takes two signals and produces a third signal. Convolution has many applications in Digital Signal Processing and Image Processing. In linear time invarient systems, convolution is used for describing the relationship between three signals, the input signal, the impulse response, and the output signal. Traditionally graphical method is used for finding convolution, which is slow and very time consuming. Vedic algorithms are used since it reduces time, increases speed and is easy to implement. This paper presents an algorithm for computing 4 bit linear convolution using vedic mathematics. The algorithm urdhva triyagbhyam based on vedic mathematics is used. The algorithm is coded in VHDL and synthesized using Spartan 6 device on Xillinx ISE simulator 14.2.

KEYWORDS*:* Linear Convolution, Vedic Mathematics, Urdhva Triyagbhyam,, VHDL.

I. INTRODUCTION

With the advancement of VLSI technology, digital signal processing plays an important role in many areas of engineering. Discrete linear convolution is an important mathematical operation which is used in many applications of image processing and digital signal processing. Convolution operation is also used for designing of digital filters. The most traditional approach for computing convolution is a graphical method. For beginners it is difficult to perform convolution because the concept and computation requires a number of steps and slow to perform. Thus direct method of calculating convolution is introduced, which is simple and it is like a regular multiplication. The principal components required for implementation of convolution calculation are adders and multipliers. Since the execution time in most DSP operations mainly depends upon the time required for multiplication operation, so there is a need of high speed multiplier. So faster vedic multipliers are used for performing multiplication operation [1].

A. CONVOLUTION

A multiplier architecture used for convolution is based on Urdhva - Triyagbhyam Sutra of Indian Vedic Mathematics is used into proposed method of linear convolution to improve its efficiency in terms of speed , area and power . This method for discrete convolution using urdhva triyagbhyam sutra of vedic mathematics is best introduced by an example. In this example, let x(n) isthe finite length sequence (1 2 4) and h(n) is the finite length sequence (1 2 3 5). The linear convolution of x(n) and h(n) is given by y(n) as [2] :

$y(n) = x(n) * h(n)$ (1)

$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$ (2)

This linear convolution can be solved by several methods developed for calculating linear convolution, resulting in the sequence y(n) = [01 04 11 19 22 20]. Here new method is used which is called direct method. This new approach for calculating the convolution sum is same as a multiplication where the convolution of x(n) and h(n) is performed as follows:

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x(n) 1 2 3 5

h(n) 1 2 4

04 08 12 20
\+ 02 04 05 10
01 02 03 06

01 04 11 19 22 20

y[1] y[2] y[3] y[4] y[5] y[6]

Fig:1: Direct method of convolution.

Fig:1 shows computation of the convolution sum, the approach is similar to a simple multiplication calculation, except here carries obtained are not forwarded to next column[2]. They are directly added in result. In this way obtained sequence is a direct result of convolution. In fig:1, y[1] to y[6] is a result of convolution operation.

B. VEDIC MULTIPLIER

Vedic mathematics is part of four Vedas. Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. They explained 16 sutras in vedic mathematics for performing different mathematical operations [4]. Out of that Urdhva tiryagbhyam sutra is used for multiplication operation."Urdhva – Tiryagbhyam Sutra" of vedic mathematics for multiplication is used to develop multiplier architecture for convolution operation. It is similar to the popular array multiplier architecture. This Sutra showseasiest way for performing multiplication of large numbers. Use of this sutra reduces computation time and complexity. Thus, whole multiplication process is simplified.

1) Urdhva-Tiryagbhyam Sutra

The multiplier used for performing convolution is based on an Urdhva Tiryagbhyam (Vertical & Crosswise) sutra of Indian Vedic Mathematics. Urdhva Tiryagbhyam Sutra is a general multiplication formula. The meaning of urdhva tiryagbhyam sutra is "Vertically and crosswise". It is based on a concept in which all partial products are generated by vertical and crosswise multiplication and result is obtained by addition of these partial products.

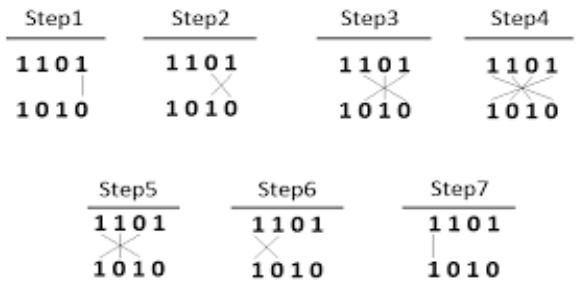

Fig 2:Steps involved in Urdhva Tiryagbhyam Sutra

As shown in fig 2, in 4 bit vedic multiplication, total 7 steps are involved. In step1, least significant bits of multiplier and multiplicand are multiplied and result is obtained. In step 2, LSB of multiplicand is multiplied with next higher bit of multiplier and it is added with multiplication of LSB of multiplier and next higher bit of multiplicand. Then obtained sum gives result and carry is forwarded to next stage. That carry is added with the sum obtained in next stage. In step 3, addition of three products is performed. Obtained result is sum and carry forwarded to next step. In next step addition

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of four products is performed as shown in fig: 2. This operation continues till MSBs of multiplier and multiplicand are multiplied. The final sum and carry is obtained. If carry is present at last stage then it is forwarded to next column and it is written as a result. In this way for four bit vedic multiplication maximum 8 samples of result is obtained using seven steps of urdhva tiryagbhyam algorithm.

II. PROPOSED WORK

For this project work, the direct method of computing linear convolution which is discussed in earlier section is implemented. The vedic multiplier for multiplication and carry look ahead adder for addition are selected. The vedic multiplier and adder are designed. The block diagram is designed for project work and it is shown below:

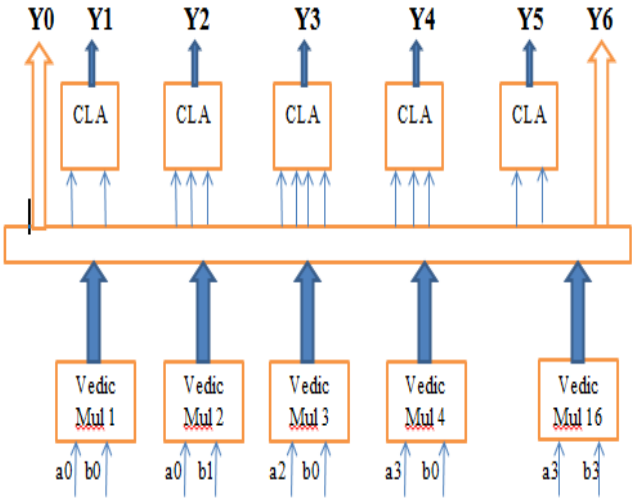

Fig 3: block diagram of four bit linear convolution using vedic mathematics

Fig 3 shows block diagram of proposed algorithm of linear convolution using vedic mathematics. a and b are inputs for convolution, each is array of four samples. The sequence Y0 to Y6 is the output sequence of convolution. For obtaining 16 partial products, 16 vedic multipliers are used. The output of each 4 bit vedic multiplier is 8 bit. As partial products are obtained in parallel manner , speed of computation is increased. For additon, different adders are studied and synthesized using xillinx ISE simulator 14.2 and CLA adder is used, which is faster one. The Y0 to Y6 is an output convolution sequence. The samples Y0 and Y6 are direct partial products. The remaining output sequence is obtained by adding partial products.

III. RESULTS

The linear convolution algorithm proposed in this paper is coded in VHDL and simulation results are obtained. The algorithm is synthesised using the xilinx design suit 14.2 with the device family as Spartan 6 and device as xc6slx16-3csg324.Two inputs given as x and h. The output is shown as y in simulation window. The table 1 below shows the synthesis report of the proposed work for convolution using vedic mathematics with the logic resource utilization.The simulation results of 4 bit linear convolution along with device utilization summary and delay comparison results is shown below:

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Device utilization	Used	Available	Utilization
Number of slices	1712	4656	36%
Number of IOBs	92	232	42%
Number of LUTs	62	9112	1%

Table 1: Device utilization summary

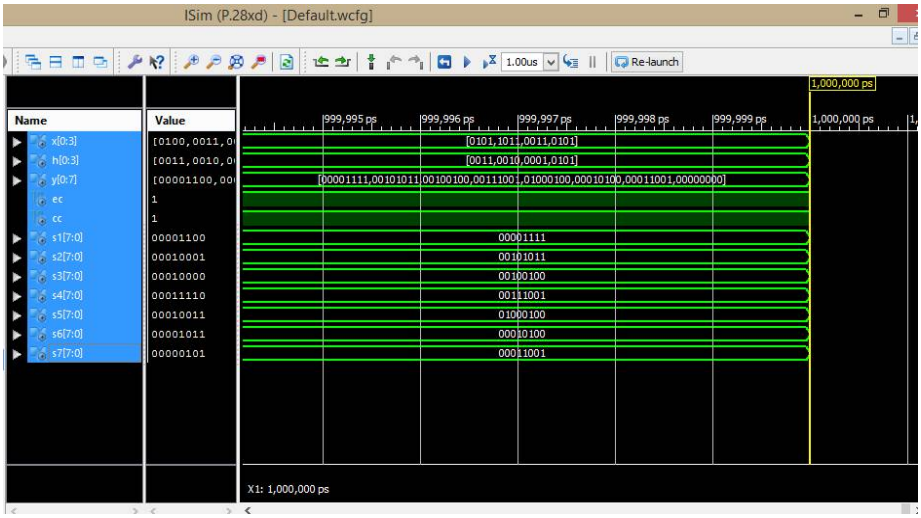

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Fig 4 : Simulation result of 4 bit linear convolution using vedic mathematics

Here, x = 0101, 1011, 0011, 0101 [05 11 03 05]
h = 0011, 0010, 0001, 0101 [03 02 01 05]

y= 00001111, 00101011, 00100100, 00111001, 01000100, 00010100, 00011001

[15 43 36 57 68 20 25]

In fig 4, simulation results of four bit linear convolution using vedic mathematics. Here x and h are input sequence and its impulse response sequence and y is a output sequence.The result of convolution obtained in simulation and calculated result of convolution are verified and both answers are matched.

Table 2 below shows delay comparison of convolution. In [3], serial implementation of linear convolution is explained. In that algorithm, only one vedic multiplier is used. Though the hardware used is less but the delay produced is more.it is upto 183.19 ns.

In my project work, parallel implementation of linear convolution is developed using fastest adder i.e. carry look ahead adder. Though parallel implementation is used, partial products are generated in parallel manner. Due to that delay introduced is much less. It is observed as 11.727 ns

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Delay of linear convolution using conventional method [3]	195.092ns
Delay of proposed method of convolution	11.727ns

Table 2: Delay comparison of convolution

IV.CONCLUSION

In This paper, an algorithm is developed for performing 4 bit high speed linear convolution with the help of urdhva tiryagbhyam sutra of vedic mathematics. The proposed algorithm is easy to learn and perform. The algorithm is coded in VHDL. The proposed method is synthesized and performed using xillinx ISE simulator 14.2 with Spartan 6 device as xc6slx16-3csg324.The advantages of the proposed architecture is efficient in speed and area. The computation time required for performing convolution operation is less as compared with the conventional method.

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