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Multi Threshold Low Power SRAM Using Floating Gates

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ABSTRACT: We investigate the mechanism of threshold voltage shifting of SRAM based on floating gates. Multi threshold SRAM based on floating gates is represented in this paper to reduce the power consumption and leakage current. By using multi threshold technique in SRAM based on floating gates, it consumes 66.39% less power for write'1' operation, 56.21% less power for write'0' operation, 23.35% less power for read'1' operation and 34.66% less power for read'0' operation as compared to SRAM using floating gates. It also consumes 90% less leakage current in hold state as compared to SRAM using floating gates in 180nM technology. For minimizing power consumption and leakage current, the concept of multi threshold is included in this paper.

KEYWORDS: Floating gate, Multi V_{th}, Transistor Stacking, SRAM.

I. INTRODUCTION

Rapid growth in VLSI fabrication process results in the increase of the densities of integrated circuit by scaling down the technology. But the devices with such high densities lead to high power consumption and run time failure. Supply voltage has been scaled down to maintain low power consumption. Hence to control drive current and to achieve high performance, transistor threshold voltage (v_{th}) scaling leads in the exponential increase of the sub threshold leakage current [1]. Static random access memory is used in most of the embedded and portable devices because of the high speed [2]. Due to the strong demand of the SRAM memory, reduction of power consumption and leakage current of SRAM memory is very important to improve system performance, efficiency and reliability [2].

The conventional SRAM is composed of two inverters connected back to back and two access transistors to connect bit lines with storage cells. Stability is also an important parameter of SRAM cell design. Stability defines how the memory cell is affected by process verification and operating conditions [3]. Stability can be measured by calculating static noise margin (SNM) , which is the maximum tolerable DC noise voltage at a storage node[3].

This thesis work focuses on reduction of static power using combine of stack and multi threshold voltage principle. Figure 1 shows the structure of stack approach. When more than one transistor in the stack is turned off, the sub-threshold leakage current of a stack of series connected transistors suppresses. This effect is called as stacking effect [1],[4]. In figure 1 when both N_1 and N_2 transistors are turned off , due to small amount of drain current, the voltage at intermediate node N (V_N) is positive. This positive voltage at intermediate node has three effects.

- Due to positive voltage at node N, the gate to source voltage (V_{GS1}) of N_1 reduces. Hence the sub-threshold current decreases [1],[4].
- Due to positive voltage at node M, the body to source voltage (V_{BS1}) of N_1 becomes negative , resulting in an increase in the threshold voltage(larger body effect) of transistor N_1 and hence reducing the sub-threshold leakage current[1],[4].
- Due to $V_N>0$, the drain to source voltage (V_{DS}) of transistor N_1 decreases. So the threshold voltage increases (less DIBL effect) which leads to reducing of sub-threshold leakage current [1],[4].

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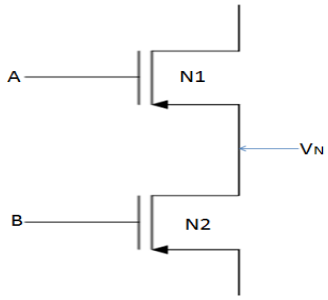

Figure 1. Stacking Approach

The stacking effect states that the circuit is far less leaky in more than one OFF transistors in the path from supply voltage to ground as compared to a circuit with one OFF transistor in the path [5],[6]. The number of OFF transistors is related to leakage power as shown in figure 2.

Multi threshold voltage CMOS technology provides both high V_{TH} and low V_{TH} transistors in a single chip to control leakage current problem [7]. The high threshold voltage transistors can reduce leakage current, while low threshold voltage transistors are used for high performance. The structure of multi V_{TH} principle is shown in figure 3.

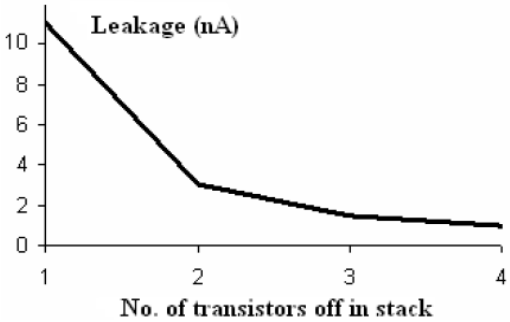

Figure 2. Transistors Stacking Vs Leakage Current

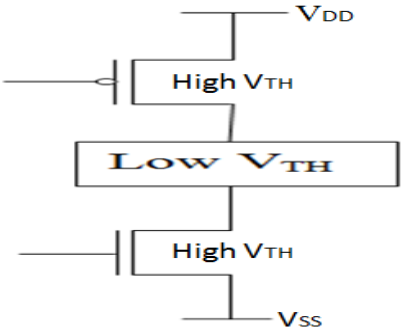

Figure 3. Multi Threshold Voltage Circuit Approach

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II. FLOATING GATE MOSFET

The floating gate MOSFET (FGMOS) is similar to a conventional MOSFET. The gate of the FGMOS is electrically isolated and create a floating node in DC [9],[10]. Multiple inputs are deposited through resistors and capacitors above the floating gate and electrically isolated from it. Floating gate MOSFET is completely surrounded by highly resistive material. So the charge stored in it remains unchanged for long period of time. Number of inputs act as floating inputs of the transistor [8],[9].

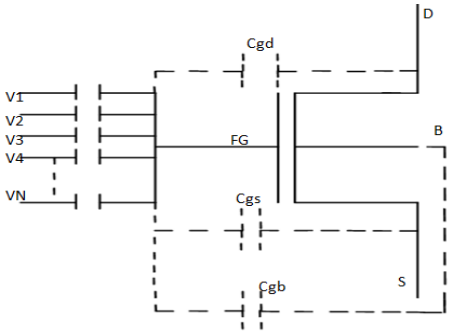

Figure 4. N channel N input FGMOS Transistor

III. SRAM USING FLOATING GATES

The SRAM using floating gate in 45nm technology is shown in figure 5. The storage node can be directly connected with bit lines through the pass transistors. Voltage deviation mainly occurs due to leakage current and damage the storage nodes [10].

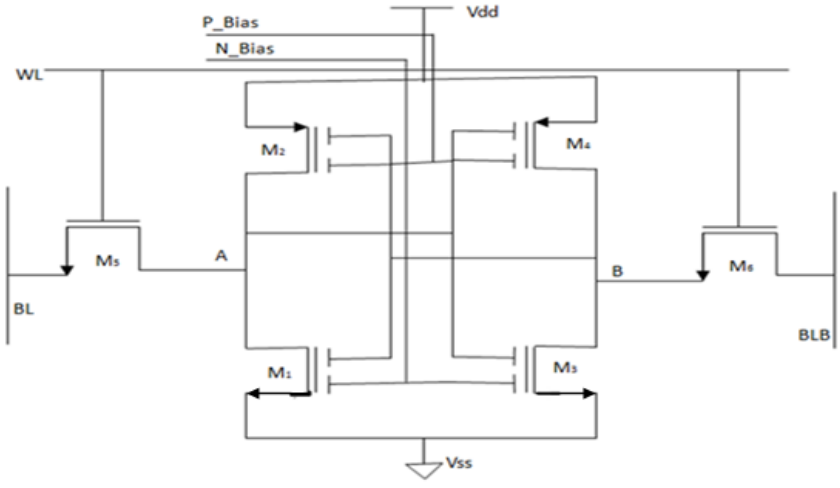

Figure 5. SRAM using Floating Gates

Sizing of the cross coupled inverters and access transistors play an important role to maintain data stability and high speed. For maintaining read stability, the cross coupled transistors M_1 and M_3 must be stronger than access transistors M_5 and M_6. For write stability, the cross coupled transistors M_2 and M_4 must be weaker than access transistors M_5 and M_6. Two input NFGMOS and PFGMOS are implemented in conventional SRAM. One of the inputs of both FGMOSs is connected with bias voltage. NFGMOS is connected with positive bias voltage and PFGMOS is connected with negative bias voltage.

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Initially BL and BLB are pre-charged by V_{DD}_Low when particular SRAM cell is not selected. In case of both read and write operation, the access transistors M_5 and M_6 are in saturation mode. For write '1' operation, BL must be 1 and BLB must be 0. When WL goes high, the access transistors M_5 and M_6 turns on and for those transistors M_2 and M_3 are on and V_{DD} value is appeared at node A. For read operation, the value which is stored at node A passes towards BL and node B passes towards BLB and sense amplifier sense the value. For write'0' and read '0' operation, the opposite phenomenon will occur.

IV. MULTI V_{TH} SRAM USING FLOATING GATES

Figure 6 represents multi V_{TH} SRAM using floating gates. The transistors M_1 to M_6 comprise the SRAM using floating gates. In both pull up and pull down network, stacking is applied. Transistors M_9 and M_{10} are connected as NMOS stacking transistors between pull down network and ground. Transistors M_7 and M_8 are connected as PMOS stacking transistors between supply voltage and pull up network.

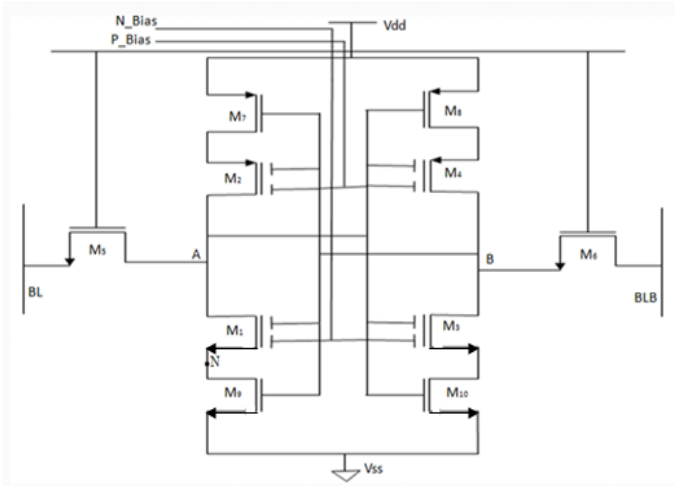

Figure 6. Multi V_{TH} SRAM using Floating Gates

During cell hold state, the node at '0' value is connected to ground through to series connected NMOS off transistors. So, leakage current reduces due to stack effect. Similarly the leakage current flowing through PMOS off transistors in pull up path also reduces due to stacking effect. The power can be reduced by using high threshold voltage transistors. In this memory cell, both high V_{TH} and low V_{TH} transistors are used. M_7, M_8, M_9, M_{10} transistors are high V_{TH} transistors. Other transistors are low V_{TH} transistors. Transistors sizing of multi V_{TH} SRAM using floating gates is same as SRAM using floating gates .

V. SIMULATION RESULTS

In this section comparison between SRAM using floating gates and multi V_{TH} SRAM using floating gates cell has been carried out on the basis of total power consumption, leakage current delay and SNM in 45nM technology.

A. Total Power Calculation

Total power consumed by SRAM cell is the sum of power drawn from supply, to charge and discharge bit-lines (BL and BLB) and word line (WL). Power consumption is calculated by multiplying the current drawn from the supply and supply voltage.

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Table 1: Percentage power improvement in the Multi V_{TH} SRAM using floating gates compared to SRAM using floating gates.

Operation	**SRAM using floating gates(µW)**	**Multi V_{TH} SRAM using floating gates(µW)**	**Improvement (%)**
Write 1	147.1	49.44	66.39
Write 0	215.5	94.36	56.21
Read 1	415.3	318.3	23.35
Read 0	349.4	228.3	34.66

Table 1 shows total power consumption of SRAM using floating gates and multi V_{TH} SRAM using floating gates and improvements in the proposed design.

B. Leakage Current

Leakage current is calculated in hold state.

Table 2: Percentage leakage current improvement in the Multi V_{TH} SRAM using floating gates compared to SRAM using floating gates.

Operation	**SRAM using floating gates(µA)**	**Multi V_{TH} SRAM using floating gates(µA)**	**Improvement (%)**
Leakage Current	82.62	8.256	90.00

Table 2 shows leakage current of SRAM using floating gate, multi V_{TH} SRAM using floating gates and improvements.

C. Delay Calculation

SRAM delay is defined as the time taken to change the node voltage from one logic to other logic.

Table 3: Delays of SRAM using floating gates and Multi V_{TH} using floating gates.

Operation	**SRAM using floating gates(ps)**	**Multi V_{TH} SRAM using floating gates(ps)**
Write 1	12.1	8.27
Write 0	6.59	7.53
Read 1	12.03	8.225
Read 0	6.53	7.52

Table 3 shows delays of different operations for SRAM using floating gates as well as multi V_{TH} SRAM using floating gates.

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D. Static Noise Margin (SNM)

Stability of the memory cell is measured in terms of static noise margin (SNM) and it is obtained by drawing and inverting the inverter characteristics [11],[12]. It is the length of the size of the maximum square that can fit into the eye of the butterfly curve.

Table 4: Percentage SNM improvement in the Multi V_{TH} SRAM using floating gates compared to SRAM using floating gates.

Operation	SRAM using floating gates(volt)	Multi V_{TH} SRAM using floating gates(volt)	Improvement (%)
Write 1	0.52	0.62	19.23
Write 0	0.1	0.12	20
Read 1	0.5	0.64	28
Read 0	0.1	0.12	20
Hold	0.48	0.66	37.5

Table 4 shows write and read stability of SRAM using floating gates and multi V_{TH} SRAM using floating gates and improvements in the proposed design.

VI. CONCLUSION

With the aim of low power and high SNM SRAM cell, this multi V_{TH} SRAM using floating gate is designed. The multi V_{TH} SRAM using floating gates consumes 66.39% less power for write'1' operation, 56.21% less power for write'0' operation, 23.35% less power for read'1' operation and 34.66% less power for read'0' operation as compared to SRAM using floating gates. It also consumes 90% less leakage current in hold state as compared to SRAM using floating gates. The above circuit is designed and simulated in cadence virtuoso environment in 180nM technology.

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