Non Isolated Single Phase AC-AC Converter Based on Adaptive Continuous Current Source Drive

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ABSTRACT: Current source drivers (CSDs) have been reduce the switching loss and gate drive loss in megahertz (MHz) dc-dc converters, in which the duty cycle normally has a steady-state value. However, different from dc-dc converters, the duty cycle of the power factor correction (PFC) converters is modulated fast and has a wide operating range during a half-line period in ac –dc applications. An adaptive full-bridge CSD is used as a boost PFC converters. The CSD can build adaptive drive current inherently depending on the drain current of the main power MOSFET. Compared to the CSDs with the constant drive current, the advantage of the adaptive drive current is reduce the switching loss further when the MOSFET is with a higher switching current, while minimizing the drive circuit loss when the MOSFET is with a lower switching current. Therefore, the adaptive CSD is able to realize better design trade-off between the switching losses and drive circuit loss so that the efficiency can be optimized in a wide operation range. Furthermore, no additional auxiliary circuit and control are needed to realize the adaptive current. A full bridge (FB) inverter at the back end of dc-dc converter completes the ac-ac conversion. This circuit enables to provide controlled and regulated ac output. The AC-AC converter is designed and simulated using MATLAB 2010 and waveforms are analysied. Simulation results demonstrate that the output voltage of the desired converter can be maintained at 349 V ac and Power factor can be improvedupto 0.909.

KEYWORDS: Interleaved Boost Converter (IBC), Current Source Driver (CSD), Power MOSFET, Power Factor Correction (PFC), Inverter

I. INTRODUCTION

An adaptive FB CSD for boost PFC converters to achieve fast switching speed and significant switching loss reduction. Compared to other CSDs with the constant drive current, the advantage of the adaptive drive current is reduce switching loss further when the power MOSFET is with a higher switching current, while reducing drive circuit loss when the MOSFET is with a lower switching current. This provides better optimal opportunity with the trade-off between the switching loss reduction and CSD drive circuit loss during a wide operation range [1]. Compared to the Resonate gate drives and CSDs can not only recover the excessive gate drive loss but also reduce the dominant switching losses in hard switching converters. An Interleaved PFC boost converter simply consists of two body converter in parallel operation 180^0 out of phase. It is used to increase the conversion energy and power conversion density and reduce ripple amplitude. The advantage of interleaved boost converter compared to the classical boost converter are low input current ripple, high efficiency, and faster transient response, reduced electromagnetic emission and improved reliability. The Interleaved boost converter has high voltage step up, reduced voltage ripple at the output, low switching losses, reduced electromagnetic interference and faster transient response. Also, the steady-state voltage ripples at the output capacitors of IBC are reduced [2]. Though IBC topology has more inductors increasing the complexity of the converter compared to the conventional boost converter it is preferred because of the low ripple content in the input and output sides. In order to reduce this complexity, this suitable IBC for both fuel cell and PV applications. In ac–dc applications, the power factor correction (PFC) technique is widely used. Different from dc–dc converters, the duty cycle of the PFC converters needs to be modulated fast and has a wide operation range. Normally, the switching loss is proportional to the switching current and the drain-to-source voltage. For a boost PFC converter,

the input line current follows the input line voltage in the same phase. When the line voltage reaches the peak value of the power MOSFET, the line current also reaches the peak and so does the drain This means that the switching loss reaches its maximum value at this moment. Output of dc-dc converter fed to single phase Full Bridge Inverter [3]. The frequency of output voltage can be controlled by varying the time period. The switching signals of full bridge inverter provided by using Sinusoidal Pulse Width Modulation (SPWM). Working of the circuit and verification by simulation results are discussed in this paper. Simulation is done in MATLAB 2010 with 110 V_{ac} input and output is 349 V_{ac} output.
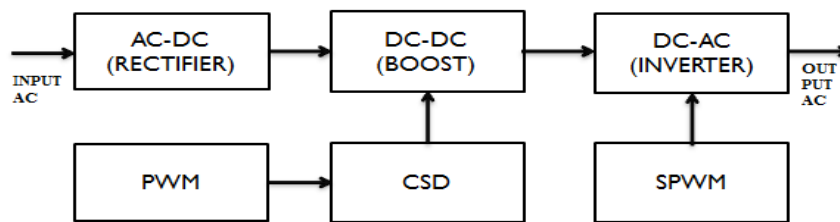

Figure 1: Schematic block diagram

II. CSD FOR A BOOST CONVERTER

The CSD circuit for the boost PFC converter is shown in Figure 2. Compared to half bridge CSD switch S_2 and S_4 are used to remove the blocking capacitor C_b, which forms a Full Bridge (FB) CSD structure [4]. Since there is no longer any blocking capacitor C_b, the CSD is be suitable for the boost PFC converters with the modulated duty cycle. It consists of four switches S_1 and S_3, and S_2 and S_4 are controlled complementarily with dead time.
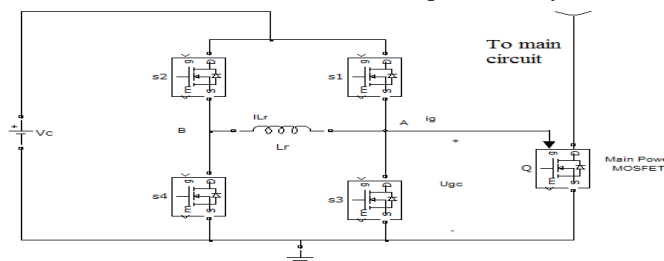

Figure 2: CSD Solution for PFC application

A. Principle of Operation

The CSD circuit for PFC application is shown in Figure 3. It consist body diodes D_1-D_4 and capacitors C_1-C_4 are the drain-to-source capacitance which are connected across the S_1-S_4, respectively C_{gs} is the gate-to-source capacitor of Q. Thereare eight switching modes in one switching period.
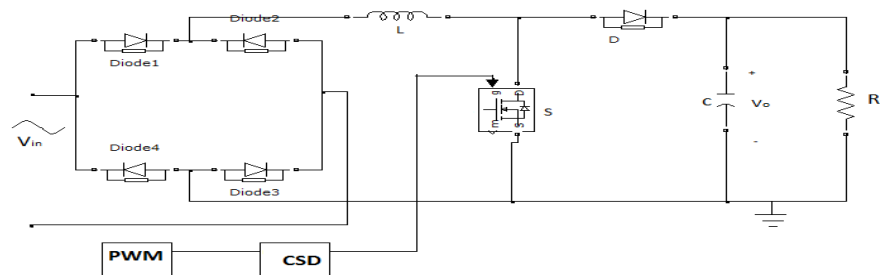

Figure 3: CSD Solution for the boost PFC converter

1) *Mode -1*:If S_3 is on and the gate of Q is clamped to ground. When S_3 is turned off, the peak value I_{peak} of the inductor current I_{Lr} charges C_3 plus C_{gs} and dischargeC_1through the Current Source (CS). Due to C_1 and C_3, S_3 achieves zero-voltage turnoff. The voltage of C_3 rises linearly and the voltage of C_1 decays linearly.

2) *Mode -2*:The body diode D_1 conducts and S_1turned ON with the zero-voltage condition. The gate-to-source voltage of Q is clamped to V_c through S_1. During this interval, I_{Lr} decreases and changes its polarity from Ipeak to -Ipeak.

3) *Mode -3*: If S_1turned OFF and the negative peak value -Ipeak charges C_1 and discharges C_3 plus C_{gs}through the as a CS. Due to C_1 and C_3, S_1 achieves zero-voltage turnoff. Then the voltage of C_1 rises and the voltage of C_3 decreases linearly

4) *Mode -4*:If D_3 conducts and S_3turned ON with the zero-voltage condition. The gate to- source voltage of Q is clamped to ground through S_3. The current path during this interval is S_3–L_r –S_4. I_{Lr} circulates through S_3 and S_4 and remains constant in this interval.

5) *Mode -5*:If S_4turned OFF and the negative peak current -I_{peak} charges C_4 and discharges C_2through the. Due to C_2 and C_4, S_4 achieves zero voltage turnoff. The voltage of C_4 rises linearly and the voltage of C_2 decays linearly.

6) *Mode -6*:If D_2 conducts and S_2turned ON with the zero-voltage condition. I_{Lr} decreases from -Ipeak and changes its polarity to I_{peak}.

7) *Mode -7*:If S_2turned OFF. The peak drive current Ipeak charges C_2 and discharges C_4. The voltage of C_2 rises linearly and the voltage of C_4 decays linearly.

8) *Mode -8*:IfD_4 conducts and S_4turned ON with the zero-voltage condition. The current path during this interval is S_4–L_r –S_3. I_{Lr} circulates through S_3 and S_4 and remains constant during this interval [1].

B. Adaptive Gate Drive Current of Power MOSFET

In mode 2, the voltage applied to the inductor V_{AB} is the drive voltage V_c. The relationship between the inductor value L_r and the peak current I_{peak} of the Current Source inductor is

$$I_{peak} = \frac{V_c * D}{2 * L_r * f} \qquad\qquad D < .05 \qquad\qquad (1)$$

$$I_{peak} = \frac{V_c * (1-D)}{2 * L_r * f} \qquad\qquad D > .05 \qquad\qquad (2)$$

Where D is the duty ratio, f is the frequency and $L_r$is the inductor.Advantages of adaptive current source drives are overall efficiency can achieve during a wide operation range, leads to a higher driver current, faster switching speed andlower switching loss.

III. INTERLEAVING BOOST PFC CONVERTERS WITH CSD

The presented adaptive CSD circuit with one inductor can drive two interleaved boost PFC converters directly as shown in Figure 4. The advantage is that only single FB CSD is required. It is noted that Q_1 and Q_2 are turned ON and OFF by the peak current of the CS inductor so that fast switching speed and switching loss reduction can be realized. In addition, S_1, S_3 and S_2, S_4 are with complementary control, respectively, and therefore, the commercial buck drivers with two complementary drive signals can be directly used to the CSD circuit. These reduce the complexity of the CSD circuit implementation with the discrete components. Other benefits of this topology include low current stress of the power MOSFETs, ripple cancellation of input current and reduced boost inductances.
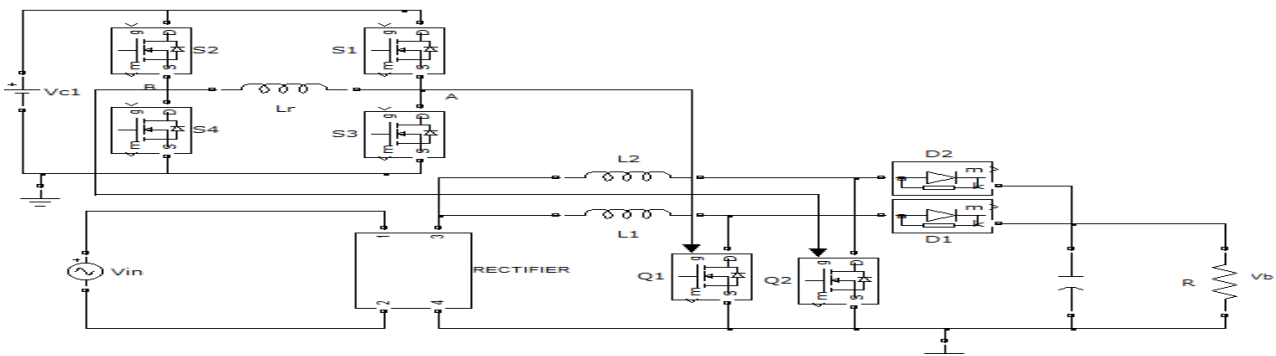

Figure 4: CSD Solution for the interleaving boost PFC converter.

IV. INVERTER TOPOLOGY

Figure 6 shows the power diagram of the single phase full bridge inverter. The inverter uses two pairs of controlled switches (T_1, T_4 and T_2, T_3) and two pairs of diodes (D_1, D_4 and D_2, D3). The devices of one pair operate simultaneously. In order to develop a positive voltage ($+V_b$) across load, switches T_1 and T_4 are tuned-on simultaneously whereas to have a negative voltage ($-V_b$) across load, we need to turn-on the switches T_2 and T_3. Diodes D_1, D_2, D_3 and D_4 are known as feedback diodes [5]

Figure 5: inverter topology.

V. SIMULINK MODEL

The main Simulink model of the system is shown in Figure 6. It consists of five subsystems. These subsystems are PWM-1, PWM-2, CSD, BOOST and INVERTER circuit model, and output signal is connected into scope. The output scope shows input voltage, boost voltage and inverter voltage across load.
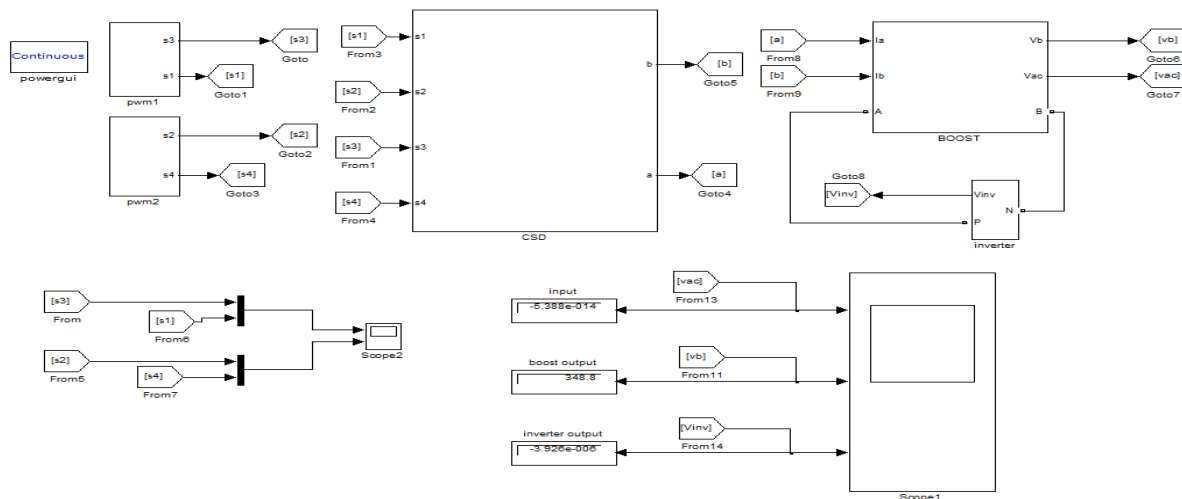.

Figure 6: Main Model

The CSD model of system is shown in Figure 7. It consists of four MOSFET and current source inductor L_r connected between the point A and B. Here L_r is 1:5μH and drive voltage is 12V.

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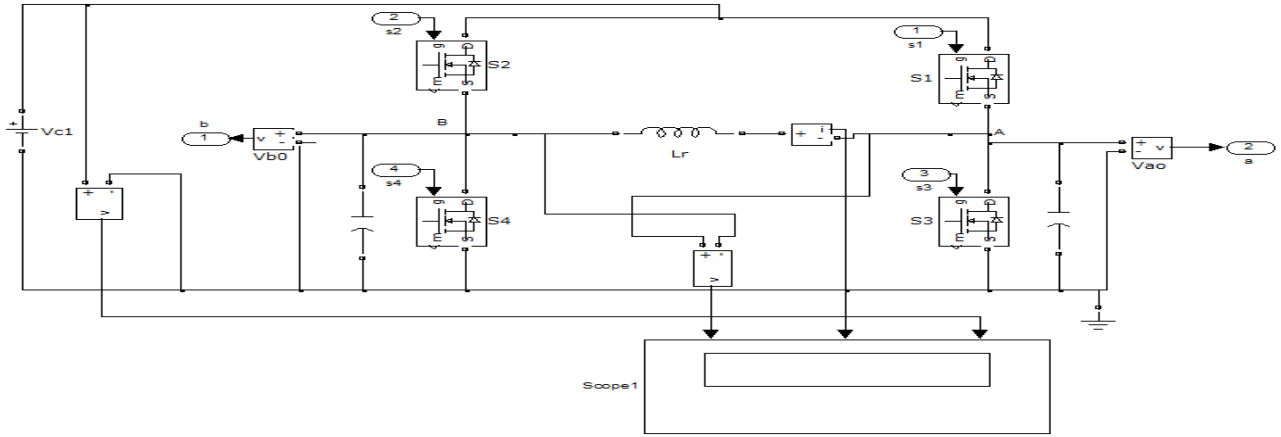## Vol. 3, Special Issue 5, December 2014

Figure 7: CSD Model

The Interleaving Boost model of the system is shown in Figure 8. It consists of two switches Q_1 and Q_2 that are connected in parallel with the same reference node, and two inductors L_1 and L_2. Here L_1 and L_2 are equal, and diodes are connected in parallel with each other. Boost inductor is $100\mu F$ and capacitor is $220\mu F$. Gate signal of Q_1 and Q_2 are coming from the CSD.
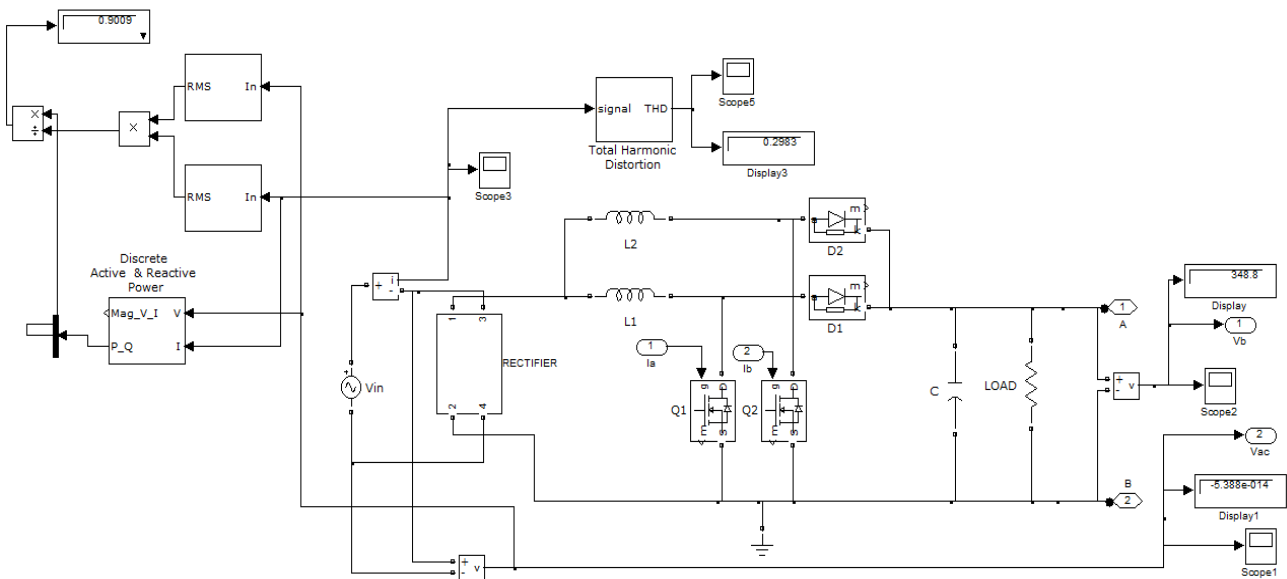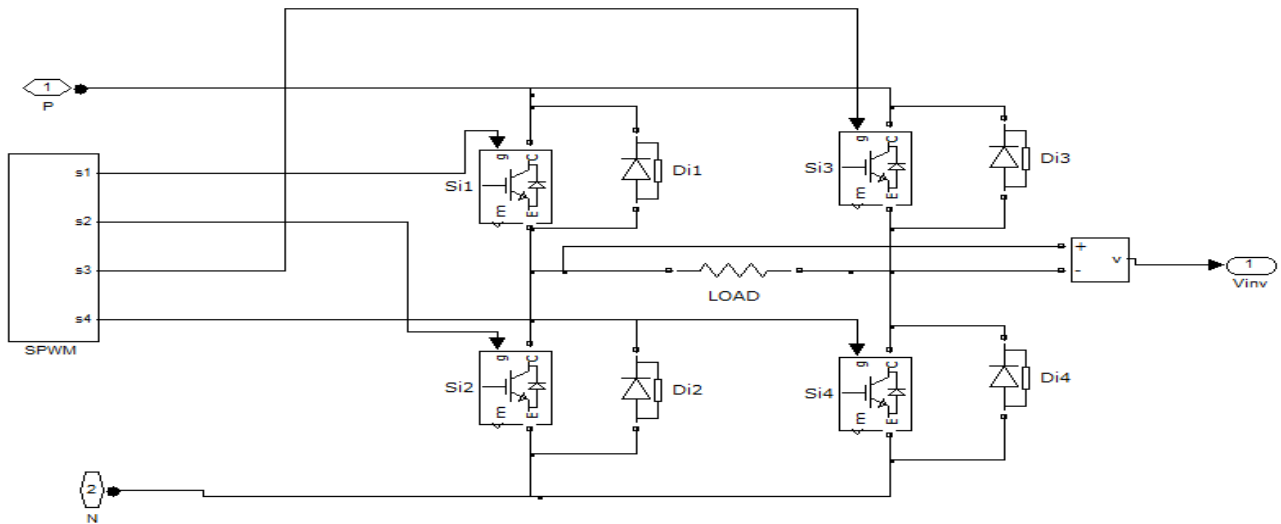

Figure 8: Interleaving Boost Model

The Inverter model of the system is shown in Figure 9. It consists of four switches and four diodes that are connected in anti-parallel for feedback. Unipolar SPWM are used for working of switch.

Figure 9: Inverter Model

VI. SIMULATION RESULTS AND ANALYSIS

For the adaptive CSD, Drive Voltage is 12 V and source current inductor L_r is 1.5μH. The input voltage is 110 V_{ac} and the output is 349 V_{ac}. The specifications for boost inductor $L = 100$ μH; output capacitance $C = 220$ μF. Figure 10(a) is the input voltage with 110V_{ac} with 50Hz frequency. The input ac voltage gets converted by rectifier and then fed toa DC-DC boost converter to get the required voltage level of 349V and it is shown in Figure 10(b). This boosted voltage is inverted into ac voltage by full bridge inverter. Figure 10(c) is output of inverter ac voltage with 349Vac.
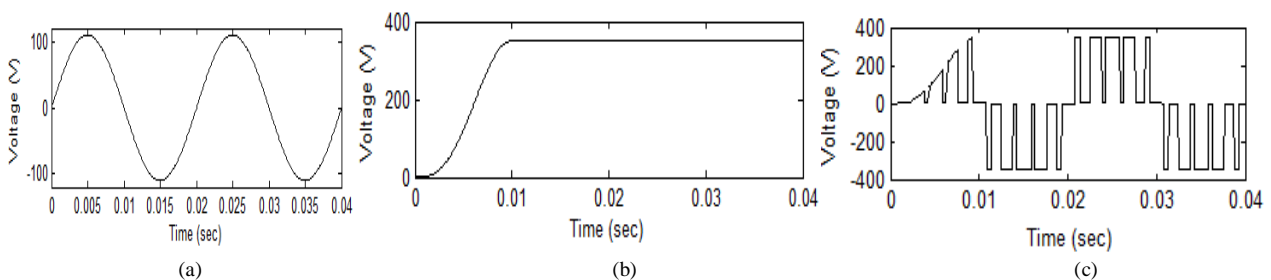

Figure 10: (a) Input voltage, (b) Boost voltage, and (c) Inverter voltage

For the adaptive CSD, Drive Voltage is 12 V and source current inductor L_r is 1:5μH. The output of the CSD model of voltage across the source inductor is shown in Figure 11(a). The output of the current through the current source inductor $I_{Lpeak}$is shown in Figure 11(b).The switches $S_1S_2S_3$ and S_4 are fed to the CSD. These switches are shown in Figure 12 (a) and Figure 12 (b).
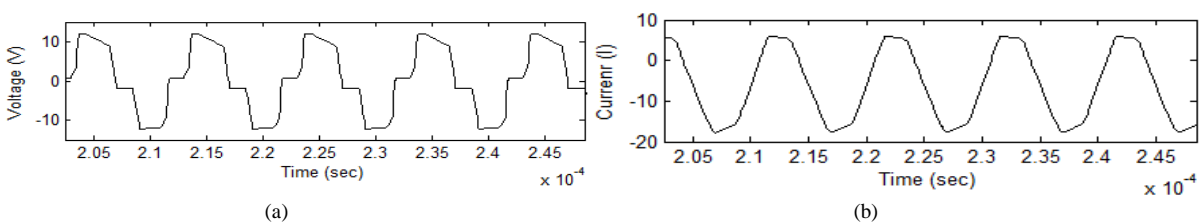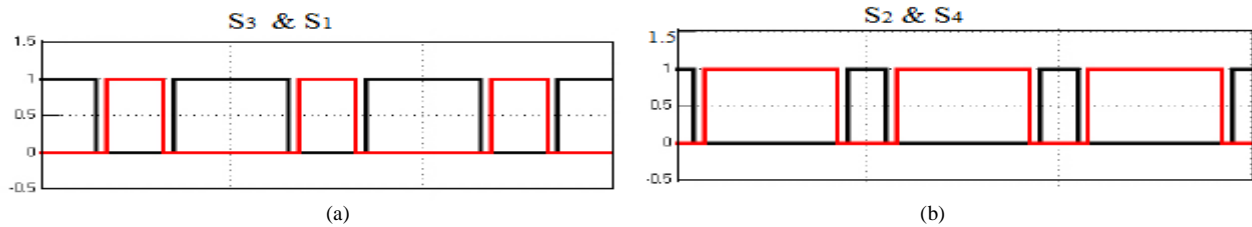

Figure 11 (a) Voltage across AB, and (b) I_{Lpeak}

Figure 12(a) S3 &S_1, (b) S2&S_4

VII.   CONCLUSIONS

An adaptive FB CSD for boost PFC converters to achieve fast switching speed and significant switching loss reduction. The advantage of the adaptive drive current can achieve further switching loss reduction when the power MOSFET is with a higher switching current while reduce the circuit loss when the MOSFET is with a lower switching current. A full bridge inverter at the back end of dc-dc converter completes the ac-ac conversion. This circuit enables to provide controlled and regulated ac output. The simulation results highlights the work done to maintain the output voltage of the converter 349 V_{ac} the circuit parameter enhance the power factor upto0.909[6].

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