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Power Efficient Comparator Architecture for Wireless Sensor Nodes

Jasmin CS[1], Angel Mathew P[2]

[1]PG Student [Applied Electronics], Department of ECE, ICET, Muvattupuzha, Kerala, India

[2]Assistant professor, Department of ECE, ICET, Muvattupuzha, Kerala, India

ABSTRACT: Designing a low power Wireless Sensor Node is highly important for getting longer lifetime. Radio transmission and data processing is energy consuming process. No compensation can be done in the field of energy consumption in radio transmission. This Paper Concentrate on energy reduction in the field of on the node processing. Due to limited energy supply from batteries the node must trade communication for on the node computation. Many of the WSN data processing algorithms uses parallel pefix operations as common denominator. Parallel Prefix Operations have the form of Binary Tree Architecture. Binary tree architecture uses more number of Processing Elements. Parallel Prefix operations using Binary Tree Architecture uses more area and more power. Binary Tree Architecture can be modified in to area and power efficient Folded Tree Architecture. A Digital comparator is a hardware electronic device that has two binary inputs and determines whether one number is greater than, less than or equal to the other number. The comparators are widely used in Micro Controller Units (MCUs) of WSN nodes. Which is a crucial data path element of image and signal processing architectures. By using Folded Tree Architecture Area and Power Efficient Comparator Architecture can be formed. Thus Power and Area efficient WSN node can be formed.

KEYWORDS: wireless sensor network (WSN), Comparator, Parallel prefix operation, Binary tree architecture, Folded tree architecture, Borrow Look Ahead Substractor (BLS)

I.INTRODUCTION

One of the primary objectives of cognitive radio (CR Wireless Sensor Networks have increasing polpularity in recent years. WSN have many practical applications including Target tracking and investigation, biomedical health monitoring, industrial inspection , hazardous environment exploration and military surveillance. A WSN contains many sensor nodes distributed over a geographical area for observing physical parameters such as temperature, pressure, humidity etc.. A sensor node is tiny device containing three important parts: a sensing subsystem for data acquirement i.e. data acquisition from the physical environment, a processing subsystem for processing and storage of data, and communication subsystem for transmission of data. With these subsystems it also contains a power source which supplies energy to the device for working and a battery. Thus, it is quite difficult to recharge the battery in unreachable environments. Designing a low power Wireless Sensor Node is highly important for getting longer lifetime. The structural view of sensor network is shown in Figure 1

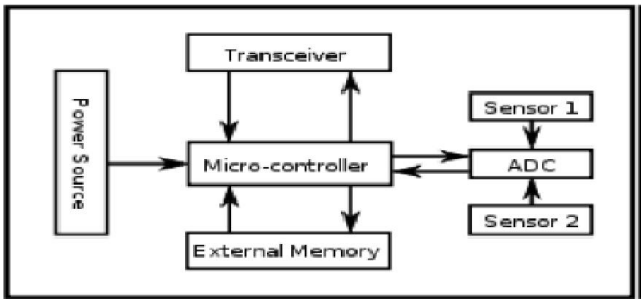

Figure 1: WSN Node Architecture.

Wireless sensor network is made up of four components: Sensing unit, processing unit, transmission unit and power
unit Sensing unit: Sensing unit consist of sensor and analog to digital converters (ADCs). Sensor convert physical phenomenon to electrical signals. The analog signals produced by sensor are converted to digital signals by ADC.

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Processing unit: The processing unit consists of microcontroller whose main task is to control sensors, execution of communication protocols and signal processing algorithms on the gathered sensor data.
Transmission unit: Transmission unit receives the information from the CPU and then transmit it to the outside world.
Power unit: In wireless sensor network, battery power is the main source of energy. So power unit regulates the battery power to sensor node

In order to make these networks a reality, the node hardware and implementation should be optimized for three Characteristics which are cost, size and power. Low cost: In order to make large scale deployments economically feasible, nodes must be of very low cost. Small size: In order to make large scale deployments economically feasible, the size of modules must be of small size . Low power: For large networks with many nodes, battery replacement is very difficult, expensive or even impossible. Nodes must have efficient energy so that it can function for long periods without running out of power.
In data intensive and computation intensive wireless monitoring application it has to pay attention in to not only demand for higher communication bandwidth and computational performance but also requires long operating life so as to reduce maintenance cost associated with replacement of batteries. Radio transmission is very energy consuming process. Due to limited energy supply from batteries the node must trade communication for on the node computation. We know that many of the WSN data processing algorithms uses parallel pefix operations as common denominator.

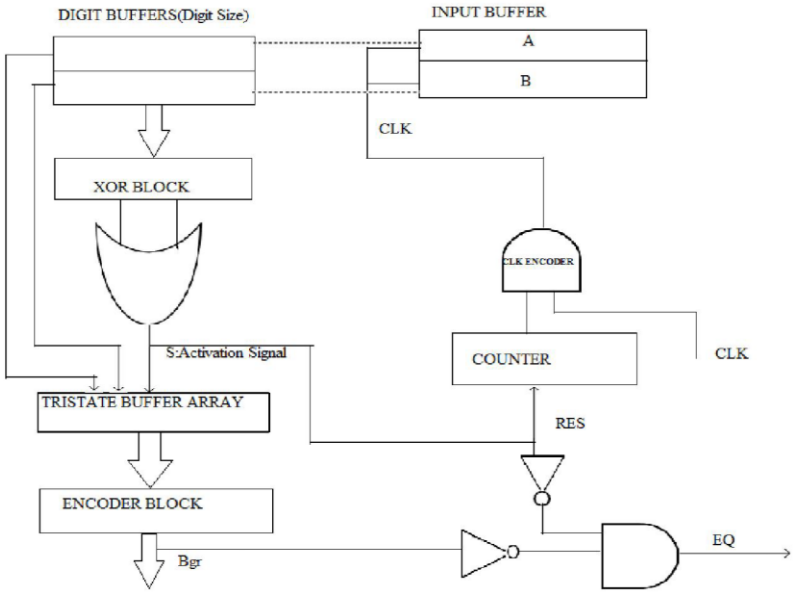

Figure 2: Block diagram of comparator.

Here we are focusing on ultralow-energy WSN digital signal processor by exploiting this and other characteristics unique to WSNs. In the traditional system binary tree architecture is used. Binary tree architecture uses more number of Processing Elements. If there is 'N' inputs these architecture requires '(N-1)' processing elements.

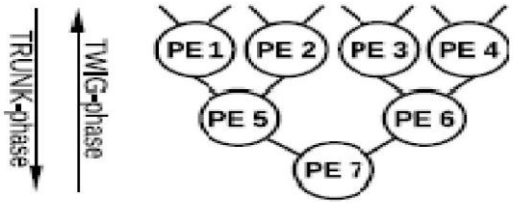

Figure 3: Binary Tree Architecture.

In order to overcome the disadvantages of binary tree architecture, Folded Tree Architecture is used. But in the folded tree architecture it uses '(N/2)' number of Processing Elements. So that we can say that Binary tree architecture uses more number of Processing Elements as compared to Folded Tree Architecture. It has high power consumption, and consume more area. Folded

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tree architecture has low number of Processing Elements and low power consumption. So the Folded Tree architecture is a low power Digital Signal Processor (DSP) architecture, which reduce the area, power than binary tree architecture.

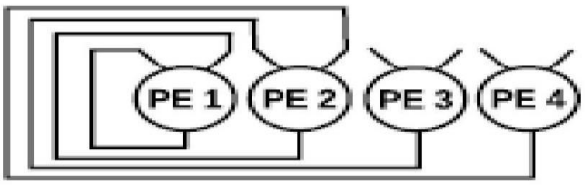

Figure 4: Folded Tree Architecture.

Digital or Magnitude Comparators are widely used in Micro Controller Units (MCU) of WSN nodes. A Digital comparator is a hardware electronic device that has two binary inputs and determines whether one number is greater than, less than or equal to the other number. Which is a crucial data path element of image and signal processing architectures. In the last few years, the design of high-speed and low power binary comparators has received a great deal of attention.
In the Proposed Binary Comparator Architecture the binary inputs are initially grouped in to digit sets .Then the digit set pair is checked for inequality. If and only if the two digit set pairs are inequal then that digit set pair taken and comparisons are made. Comparison made using BLS(Borrow Look Ahead Substractor) Principle. BLS uses Folded Tree Architecture in Calculating the Borrow. Grouping in to digit sets and usage of BLS principle make the Comparator as a High speed and Power Efficient Binary Comparator for WSN Nodes.

II. PROPOSED WORK

In the proposed work we are focusing on Low power and high speed Comparator. Low power architecture is formed by usig Folded Tree Architecture in BLS (Borrow Look Ahead Substractor) .High speed Architecture is formed by using Digit set grouping.
In the Proposed Binary Comparator Architecture the binary inputs are initially grouped in to digit sets .Then the digit set pair is checked for inequality. If and only if the two digit set pairs are in equal then that digit set pair taken and comparisons are made. Comparison made using BLS (Borrow Looh Ahead Substractor) Principle. BLS uses Folded Tree Architecture in Calculating the Borrow. Grouping in to digit sets and usage of BLS principle make the Comparator as a High speed and Power Efficient Binary Comparator for WSN Nodes Proposed Binary Comparator Block diagram is given. Proposed Comparator has two units, Pre-Computation Unit and Encoder Block. Pre-Computation unit has Input Buffer, Digit Buffer, T ristate Buffer Array CLK Encoder and Counter. The basic principle of Comparator is to group the binary inputs into digit sets .Digit size = word size/m, where m : being the number of digits formed and it is an even number. The digit sets are send to the pre-computation unit starting from Most Significant Digit (MSD) to check for equality .Computations in pre-computation unit are stopped at the first digit set which produces a "1" output. The corresponding digit set is send to the encoder block which uses BLS principle in Calculating the Borrow to find the greater of the two inputs. Proposed design avoids unnecessary checking of all the bits in the input.

2.1. Pre-computation Unit

In pre-computation unit, the Input Buffer stores the two binary inputs. Based on the digit size the counter value is initialized. For each tick of the counter the bits are shifted into the Digit Buffer (DB) from the Input Buffer. The required number of bits are shifted into the DB when the counter output reaches "0".The pre-computation unit performs EX-OR operation on bits in DB starting from Most Significant Bit (MSB). The EX-OR outputs are OR- ed to find the equality within digits. If two digit sets are equal the OR-ed output will be zero and the next digit set will be passed to the DB for comparison. In case of unequal digit sets, OR-ed output will be "1" then the computations in the pre-computation block are stopped. The corresponding digit sets are send to the encoder block to determine the greatest of the two .If the output EX-OR is zero for all digit sets, then the input word is considered to be equal. It can be realized by a "1" output at "EQ".

2.2. Encoder Block

It calculates greatest among the two inputs. It uses borrow generation equation of BLS to find the greatest among the two inputs. In case of "N" bit input "N" bit BLS is considered .BLS with Folded Tree Architecture Consume less Area and Power as Compared to BLS with Binary Tree Architecture.

$$B_{GR} = B_{out} = \overline{A_i} B_i + \left(A_i XORB\right)_i B_{i-1}$$

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$$B_{out} = B_i = F(\mathrm{G_i}, \mathrm{P_i}, B_{i-1})$$

$$B_i = \mathrm{G_i} + \mathrm{P_i}\, B_{i-1}$$

$$\mathrm{G_i} = \overline{A_i} B_i$$

$$\mathrm{P_i} = A_i XOR B_i$$

$$B_{GR} = \overline{A_7} B_7 + (A_7 XOR B_7) B_6$$

$$B_{GR} = \overline{A_5} B_5 + (A_5 XOR B_5) B_4$$

$$B_{GR} = \overline{A_3} B_3 + (A_3 XOR B_3) B_2$$

$$B_{GR} = \overline{A_1} B_1 + (A_1 XOR B_1) B_0$$

The above equations represent the Borrow Calculations done by BLS. The equation of BLS has the Parallel Prefix nature. Parallel Prefix nature can be represented by two architectures, namely Binary and Folded Tree Architecture. Folded Tree Architecture is Area and Power efficient as compared to Binary Tree Architecture. By using Folded Tree Architecture Power and area efficient Comparator Architecture can be formed.

III. ILLUSTRATION OF PROPOSED METHOD

Consider two binary inputs A and B where

A = 10110110
B = 10111010

Case 1: 2 bit digit set grouping

Here A and B are grouped and compared as follows.

- ✓ Digit set A = 10 | 11 | 01 | 10
  B = 10 | 11 | 10 | 10
- ✓ Precomputation unit

  Output "S" 0 0 1 0
- ✓ Encoder input 01
  10

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✓ Encoder output

"BGR" 1

B greater than A

Case 2: 4 bit digit set grouping

Here A and B are grouped and compared as follows.

✓ Digit set A = 1011 | 0110
B = 1011 | 1010

✓ Precomputation

unit output "S" 0 1

✓ Encoder input 01 | 10
10 | 10

✓ "Bout" 1 0

✓ Encoder output

"BGR" 1

B greater than A

IV. EXPERIMENTAL EVALUATION

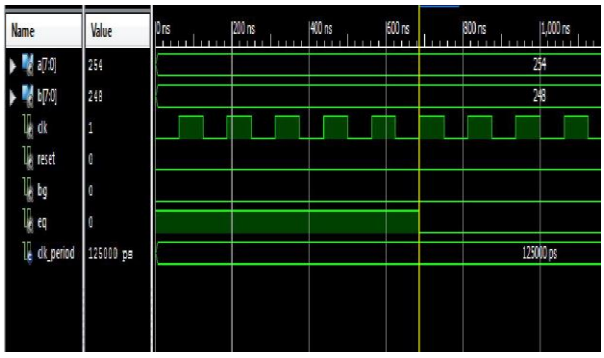

Figure 5: Output of comparator using Binary Tree Architecture.

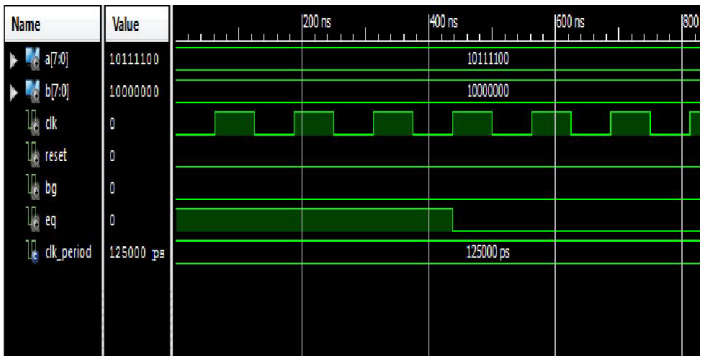

Figure 6: Output of Power efficient Comparator Arcitecture using Folded Tree Architecture

Specification	Binary Tree	Folded Tree
Area (Number of 4 input LUTs)	54	52
Power (On-chip Logic Utilization)	51	49

Table 1: Power and Area Comparison of the Proposed Comparator.

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Hardware implementation of this architecture is done by using Spartan 3E FPGA .XCS3250E FPGA is used here. In this implementation each logic is implemented using CLB (Configurable Logic Blocks).Each CLB consist of 4 slices. Each Slice will have 2 LUT (Look Up Table)s and 2 Latch /Flip Flops. LUT is used to implement the logic and Latch/FF represent memory utilization .So in Area calculation Number of LUTs will give area of that logic. In the above Table1 we can see that Binary Comparator which uses Binary Tree Architecture has more number of LUTs as compared to Comparator which uses Folded Tree Architecture. Power Utilization in Spartan 3E FPGA implementation is represented in terms of On-Chip Logic Utilization. The architecture having more On-chip logic utilization consume more power as compared to the architecture having lower On-chip logic utilization. So from Table1 we can see that Binary architecture Comparator has more power Consumption as compared to Folded Tree Architecture comparator .From above Table1 we can say that Comparator using Folded Tree Architecture is Power Efficient Comparator.

V.CONCLUSION

Power efficient Binary Comparator is implemented using Folded Tree Architecture. Usage of Digit set grouping among the two inputs and comparison of input group which possess inequality make the comparator as a high speed comparator. Comparator with Binary Tree Architecture has more number of processing elements and consume more area and more power .Comparator with Folded Tree Architecture has lower number of processing elements and has advantages including reduced area and lower Power Consumption. Thus High speed ,Power and Area efficient Comparator Architecture fow WSN Node can be formed.

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