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REDUCTION OF PAPR USING PTS AND SLM OF OFDM TRNSCIEVER SYSTEM

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ABSTRACT: This paper proposes the physical layer design and architecture of Software Defined Radio (SDR). In this SDR the OFDM (Orthogonal frequency Division multiplexing) technique BPSK or 16 QAM is used as modulation. The modulations can be selected according to the signal to noise ratio. The peak to power average ratio can be reduced by dividing the input bits as Partial Transmit Sequence (PTS). The divided bits can be selected by using selective mapping (SLM). The size of FFT is scalable and can be select according to the size transmission bits. The re-configurability of FPGA allows the receiver to select the modulation at run time without changing the current program. The run time reconfiguration reduces the complexity in modification..

Keywords: SDR, Run time Reconfiguration, OFDM, BPSK, QPSK, PAPR reduction algorithms

I.INTRODUCTION

According to the advances in the technologies in wireless communication, the customer needs also increased to communicate in any place with different accessories. The advances in the wireless communication lead to evolution of very efficient radio receivers. Software defined Radio affords an attractive nature of reconfigurable and multimode operations.

SDR is a collection of Hardware and software in which all the radio functions can be implemented using software coding or firmware on a processing system. These software can be alterable according to the applications in communication system. The processing systems include Field Programmable Gate Arrays (FPGA), Digital Signal Processors (DSP), General Purpose Processors (GPP), Programmable System on Chip (SoC) or other Application Specific Programmable Processors [1]. The use of SDR technologies allows new wireless features like Third Generation (3G) and Fourth Generation (4G) capabilities to be added to existing Generation for mobile applications and radio systems without requiring new hardware.

Software defined radio (SDR) – an idea of moving hardware components into software – helps reducing the complexity of radio devices. There are many advantages of migrating into software, including better functionality, lower manufacturing costs, smaller device dimensions together with lower power consumption, and usually greater quality, since DSP algorithms are not subject to parasitic effects in the way the hardware parts are. But there are still more advantages. The software allows for flexibility and reconfiguration [2].

By using SDR Technique a family of Radio products used in communication to be developed in common platform architecture and lot of research work is going on in this area allowing new products will come quickly into market. Since the software to be reused across radio products, the development cost reduces dramatically. This type of wireless communication enables the user to communicate with whomever they need to communicate and in whatever manner according to their wish. For example video call is available in Third generation. Likewise any type of applications can be include using SDR in a single chip. The main advantage SDR engineers is to provide a single radio transceiver capable of playing the roles of cordless telephone, cell phone(GSM and CDMA),

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II.ARCHITECTURE

By using SDR Technique a family of Radio products used in communication to be developed in common platform architecture and lot of research work is going on in this area allowing new products will come quickly into market. Since the software to be reused across radio products, the development cost reduces dramatically. This type of wireless communication enables the user to communicate with whomever they need to communicate and in whatever manner according to their wish. For example video call is available in Third generation. Likewise any type of applications can be include using SDR in a single chip[10][11].

As shown in the block diagram, we have proposed a SDR architecture with only FPGA due to the availability of massive parallelism and Partial Reconfigurable ability. Since the newer FPGA provides PR modules, it is possible to change of the certain part of FPGA alone and hence we can avoid complete FPGA for reconfiguration. The embedded PowerPC and DSP slices can do a work of a GPP or DSP. Hence it is also not required to use dedicated

In most cases DSP is used because the combination of controlling ability and signal processing power. The different demodulation techniques configuration will be loaded into a memory unit initially.

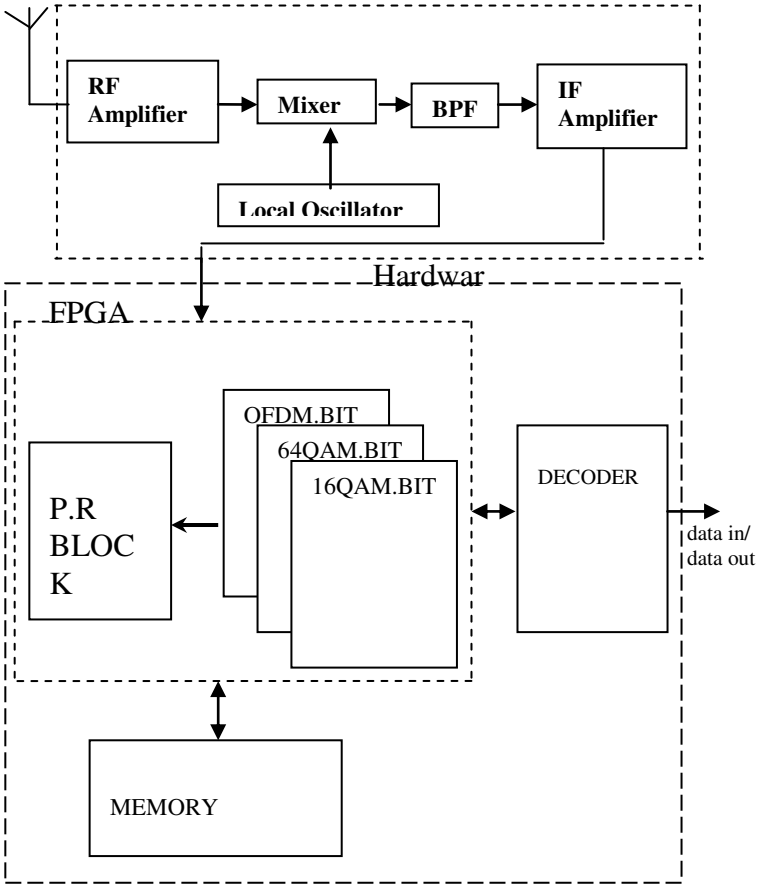

Figure 1: Architecture

Orthogonal frequency-division multiplexing (OFDM) is the modulation technique for European standards such as the Digital Audio Broadcasting (DAB) and the Digital Video Broadcasting (DVB) systems. As such it has received much attention and has been proposed for many other applications, OFDM is a type of multichannel modulation that divides a given channel into many parallel sub-channels or subcarriers, so that multiple symbols are sent in parallel.

The order (M) of the entire OFDM signal is the sum of the orders of each subcarrier, representing the total number of states available to the OFDM signal. For OFDM with N subcarriers we have

$$M_{OFDM} = N. N_{QAM}$$

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III. RE-CONFIGURABILITY

The static logic remains functioning and is completely unaffected by the loading of a partial bit file. The reconfigurable logic is replaced by the contents of the partial bit file. There will be a Configuration controller which is part of the static module. This takes care of loading and unloading of dynamic modules. The command to this controller will be given from PowerPC with the reconfiguration data[8][9].

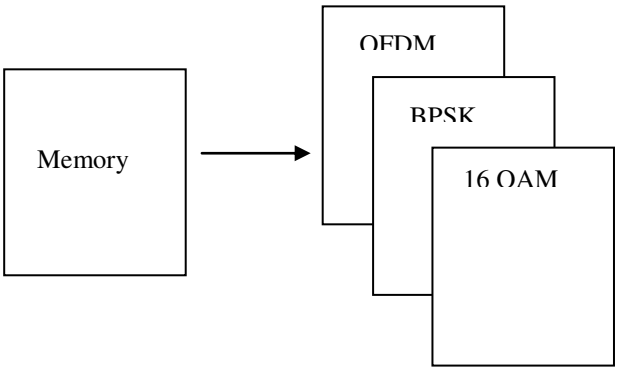

Figure2: Partial Reconfiguration

The above diagram shows the BIT files in partial reconfigurable (PR) block in FPGA. The BIT files can be stored in this as OFDM.BIT, QAM.BIT and BPSK.BIT. The Bit files can be select according the SNR value.

IV. OFDMA

Orthogonal frequency-division multiplexing (OFDM) is a transmission technique that modulates multiple carriers simultaneously. Although their spectra overlap, the transmitted multiple carriers can be demodulated orthogonally, provided that correct time windowing is used at the receiver. Since the OFDM-based system has high spectral efficiency and is robust against intersymbol interference and frequency-selective fading channels, it has been widely chosen for European digital audio/video broadcasting and wireless local/ metropolitan area network standards, and now, it is used in most broadband wireless communication systems[4].

In OFDM the modulation used on each subcarrier is QAM, and there is no filtering used on the individual subcarriers. For each OFDM symbol the data is distributed among the subcarriers: 2 bits each when 4-QAM is used; 6 bits each if 64 QAM is used. The OFDM time waveform is the sum of the magnitude and phase scaled subcarrier sinusoids at each frequency used. Since all subcarriers use the same symbol time, the OFDM waveform also has this symbol time.
One of the severe drawbacks with OFDM systems, however, is the high peak-to-average power ratio (PAPR) of transmitted signals. The high PAPR introduces inter-modulation distortion and undesired out-of-band radiation due to the nonlinearity of the high power amplifier (HPA). The distortion and radiation cause degradation of the bit error rate (BER) and high adjacent channel interference, respectively. Therefore, it is desirable to reduce the PAPR of an OFDM signal[12].

The PAPR is given by the equation

$$\text{PAPR} = \frac{P_{peak}}{P_{average}}$$

Where, P_{peak} is the Peak power of the OFDM signal and
$P_{average}$ is the average power.

The FFT of the can be calculated by using Decimation in Time, Radix 2 algorithm. Then using two SLM we can select the Signal with minimum PAPR in each FFT samples.

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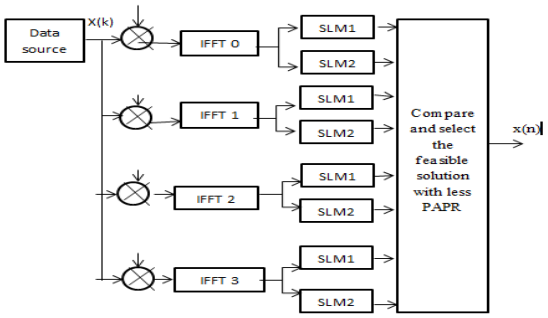

Figure3: OFDM System for IFFT calculation

The above system the information signal from the receiver X(k) is divided into four equal parts as $X_1(k)$, $X_2(k)$. $X_3(k)$. $X_3(k)$. after the division the two ifft will be calculated and find out the PAPR ratio. Finally select the signal with less PAPR ratio in the receiver $x_1(n)$, $x_2(n)$, $x_3(n)$, $x_4(n)$ and combined the four ifft will get the signal x(n).

$$\text{PAPR} = \frac{\max\limits_{0 \le t \le T} x(t)|^2}{\sigma^2}$$

Where, x(t) is the input signal from the Centre.

After finding the FFT it can be denoted as x(n). The FFT can be scalable, N can be 64, 128, 256, 512, 1024 and 2048. Any filtering used to smooth out these waveform discontinuities necessarily distorts each OFDM symbol waveform. And since the OFDM waveform is generated solely from the data on each subcarrier, any filtering distortion increases EVM. OFDM is not nearly as tolerant of EVM as filtered QAM signals are, as noted from comparing their respective EVM specification limits: 3% for OFDM, 10% or more for QAM[13].

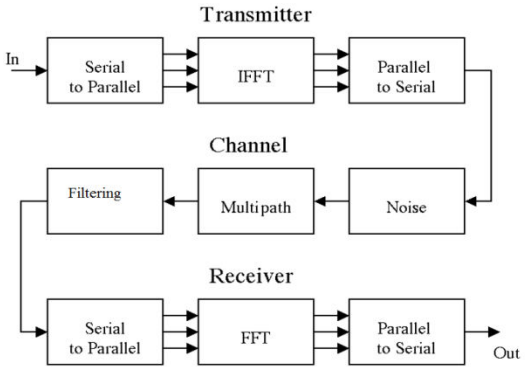

Figure4: OFDM System Architecture

The modulation used in this are BPSK and 16-QAM. The number of inputs is divided into four. Here Four IFFTs are used to reduce the PAPR. But by division the speed will be reduced. This can be rectified by using parallel processing. Cyclic prefix acts as a buffer region where delayed information from the previous symbols can get stored. The receiver has to exclude samples from the cyclic prefix which got corrupted by the previous symbol when choosing the samples for an OFDM symbol. Typically, cyclic prefix duration is determined by the expected duration of the multipath channel in the operating environment.

$$x(n) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} X(k) e^{j2\pi nk/N}$$

Where, n= 0, 1, 2 ……N-1.
x(n) is the information signal.
N is the number of samples.

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BPSK : BPSK is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, and in this figure they are shown on the real axis, at 0° and 180°.

$$s_n(t) = \sqrt{\frac{2E_b}{T_b}}\cos(2\pi f_c t + \pi(1-n)), n = 0, 1.$$

Where s(t)is the modulated signal.

QAM:- 16 QAM : 16-state quadrature amplitude modulation have four I values and four Q values yielding four bits per symbol. It has 16 states because $2^4 = 16$. The theoretical bandwidth efficiency is 4 bits/ second/Hz. Data is split into two channels, I and Q, each channel can take on two phases. The in phase and quadrature can vary separately. However, 16-QAM can accommodate two intermediate amplitude values. Two bits are routed to each channel simultaneously. The two bits for each channel are added, then applied to the respective channel modulator.

$$S_m(t) = \sum_m \left(A_m e^{i\theta_m}\right) g(t - mT) e^{i2\pi f_c t}$$

$$= A_m g(t)[\cos(2\pi f_c t + \theta_m) + \sin(2\pi f_c t + \theta_m)$$

Where , $A_m = (A_I^2 + A_Q^2)^{1/2}$.

A_I, A_Q ⟶ amplitudes of Information signal and Quadrature carriers.

g(t) ⟶ the signal pulse

θ_m ⟶ indicates phase modulation has value

$\theta_m = \tan^{-1}\frac{A_Q}{A_I}$

The state of the QAM are scalable in nature. So the state can selected according to the application and the feature size. The state can be 4, 16, 32,64, and 128. If you recall, in the post on BER computation in AWGN, the probability of error for transmission of either +1 or -1 is computed by integrating the tail of the Gaussian probability density function for a given value of bit energy to noise ratio E_b/N_o .The theoretical bit error rate for BPSK modulation

$$P_{b,BPSK} = \frac{1}{2}erfc\left(\sqrt{\frac{E_b}{N_0}}\right)$$

According to the bit error rate we can select the modulation. If the system is transmitted with high bit error rate receiver send a feedback signal to change the modulation type and resend the message again.

IV. RESULTS

The Simulation is done by using Xilinx system generator and Matlab. The Synthesis is done by using Xilinx ISE Software. The Simulation results are shown in the figures. The Modulation can be selected at the receiver according to the features. This features are extracted by adding white noise to the channel.

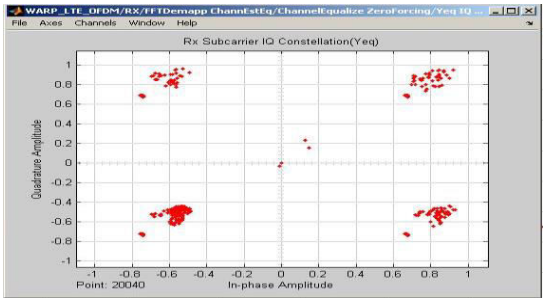

Figure 5: Constellation

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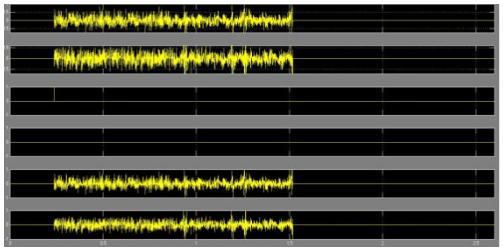

Figure 6: OFDM Signal with 64QAM

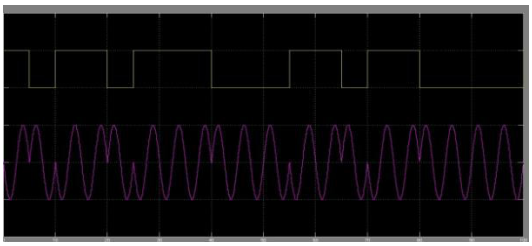

Figure 7: BPSK modulation

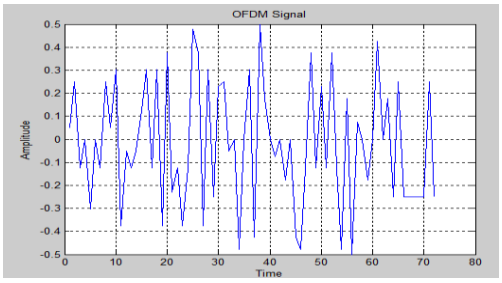

Figure 8: OFDM signal with QPSK

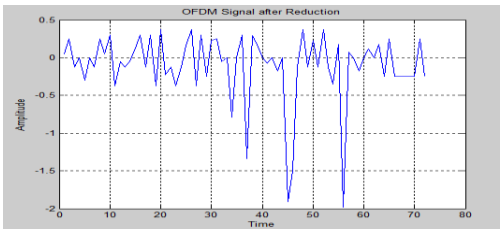

Figure 9: OFDM signal after power reduction

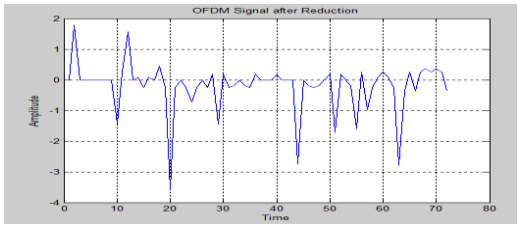

Figure 10: OFDM signal with BPSK

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V. CONCLUSION

Realization of SDR Developed by using Xilinx FPGA. Due to the Realization is done by using the help of run time Reconfiguration, the flexibility and performance can be improved. The area also can be decreased. The New Xilinx, Vertex Series FPGA provides the provision of Partial Reconfiguration. The PAPR can be reduced by using Partial transmit sequence.

This SDR Receiver can be used for military application and 4G wireless communication. The use of run time reconfiguration helps to change the coding according to the application. For future work the optimization algorithms like Genetic algorithm can be used for are and power minimization.

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BIOGRAPHY

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