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SPWM Control Strategy for Multilevel Inverter Fed an Induction Motor Drive

Bandi Naga Surendra[1], Murali Dasari[2], T.Ravi kumar [3]

PG Scholar, M.Tech (Power Electronics), GIST, Nellore, AP, India[1]

Assistant professor, Dept.of EEE, GIST, Nellore, AP, India[2]

Associate Professor, Dept of EEE, GIST, Nellore, AP, India[3]

ABSTRACT: This paper deals the control of a multilevel inverter fed with an Induction motor supplied by a Photovoltaic (PV) panel and a batteries bank. With the increase in number of levels the power quality of multilevel inverter signal may depends. However, in this paper solve the problem of how many number of levels necessary to increase for harmonic reduction. The harmonics content of the output signals are analyzed by comparing the different levels of diode-clamped multilevel inverter is shown. A sinusoidal Pulse Width Modulation (SPWM) method for a multilevel inverter that supplied an induction motor is developed. The controller equations are such that the SPWM pulses are generated automatically for any number of levels. The effectiveness of the propose method is evaluated in simulation. Matlab/Simulink is used to implement the control algorithm and simulate the system.

KEYWORDS: Induction motor, Multilevel inverter, Multilevel SPWM, THD

I.INTRODUCTION

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application.

The concept of multilevel converters has been introduced since 1975[1].The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources.

The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. Among the control algorithms proposed in the literature in this field [3-4-5], the SPWM, appears most promising. It offers great flexibility in optimizing the design and it is well suited for digital implementation. It also helps to maximize the available power.

The main advantage of multilevel inverters is that the output voltage can be generated with a low harmonics. Thus it is admitted that the harmonics decrease proportionately to the inverter level. For these reasons, the multilevel inverters are preferred for high power applications [6-7]. However, there is no shortage of disadvantages. Their control is much more complex and the techniques are still not widely used in industry [8-9]. In this paper, modelling and simulation of a multilevel inverter using Neutral-Point-Clamped (NPC) inverters have been performed with motor load using Simulink / MATLAB program. In the first section multilevel inverter control strategies are presented before to detail a study of *nine-level* inverter in the second section. Total Harmonic Distortion (THD) is discussed in the third section.

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The aim is to highlight the limit at which the multilevel inverters are no longer effective in reducing output voltage harmonics.

II. MULTILEVEL INVERTER CONTROL STRATEGIES

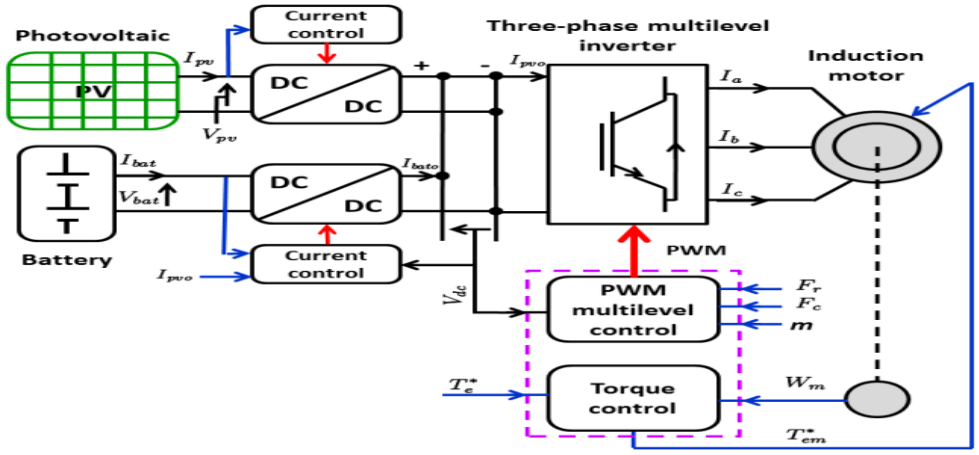


Fig. 1: Induction motor driven by PV-batteries standalone system using a controlled multilevel inverter

A. The three-level inverter control strategy:

A three-phase three-level inverter is shown in fig (2). The circuit consists of three arms. Each arm has four switches. Every switch is connected in anti-parallel with a diode. Here it describes the operation of three possible combinations for each one leg as shown in fig (3). The voltage V_{ao} between the phase "a" and the neutral point O is defined entirely by the switches position (0 'open' or 1'closed'). Switch sets [S_{11}, S_{12}], and [S_{13}, S_{14}] have complementary positions. When [S_{11}, S_{13}] are open [S_{12}, S_{14}] are closed. The three-level NPC inverter is mostly used for medium-voltage high-power applications [11].In this converter, the number of commutation sequences (Seq) is equal to 2^4= 16., where 4 stands for the number of switches per arm and 2 is the number of state per switch (0, 1).V_{dc} is the DC-bus voltage. Only three commutation sequences are possible. They are represented at Table 1.

Fig. 3 shows the configurations of the inverter's arm which correspond to the three possible commutation sequences:

- Sequence 1: S_{11}, S_{12}conduct and S_{13}, S_{14} open (Fig.3.a). V_{ao}= +V_{dc}/2.
- Sequence 2: S_{11}, S_{13} conduct and S_{12}, S_{14} open (Fig.3.b). V_{ao} = 0.
- Sequence 3: S_{13},S_{14} conduct and S_{11},S_{12} open (Fig.3.c). V_{ao} = − V_{dc} /2.

Sequences 1, 2 and 3 are applied in this order periodically.

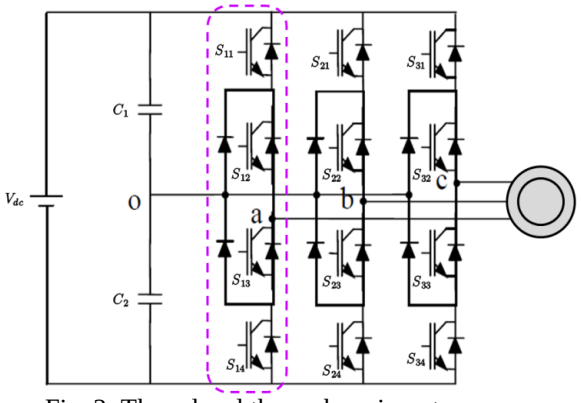
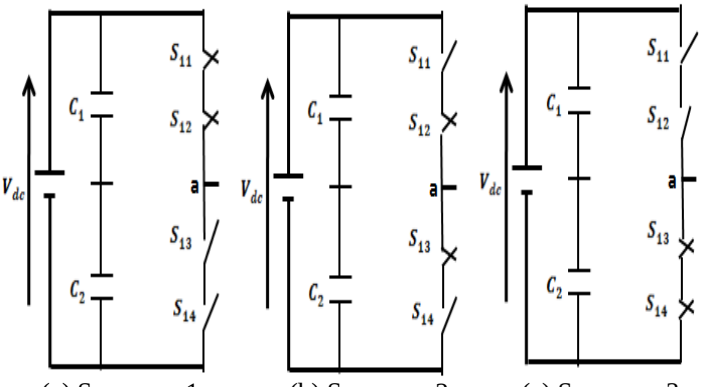


Fig. 2: Three-level three phase inverter



(a) Sequence 1 (b) Sequence 2 (c) Sequence 3

Fig. 3: Different possible configurations for one arm

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A pulse width modulation is used to control the switches Consider Fig. 4 and Fig. 5, the reference voltage V_{ra} compared to the positive and negative sawtooth carrier V_{cx} and V_{cy} respectively. The comparator output is sent to the switches (Insulated Gate Bipolar Transistor or IGBT) to generate the machine phase voltage.

The modulated SPWM voltage has the following characteristics:
- SPWM pulses frequency is the same as the sawtooth carrier f_c. The magnitude is 1 ($f_{SPWM} = f_c$,)
- the fundamental frequency is controlled by f_r which is the same as the reference voltage V_{ra} frequency.

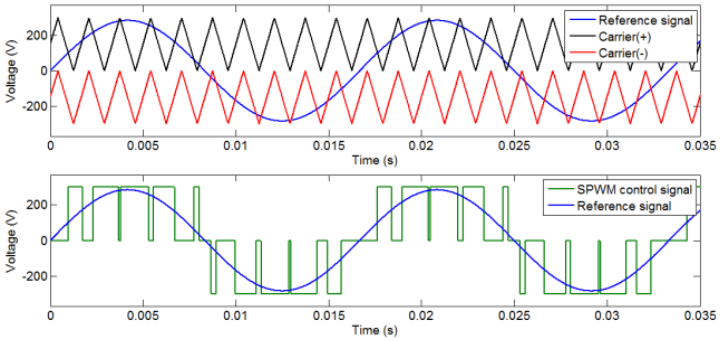

Fig. 4: Three-level SPWM control method

S.no	[S_{11} S_{12} S_{13} S_{14}]	V_{ao}
1	[1 1 0 0]	$V_{ao} = V_{dc}/2$
2	[0 1 1 0]	$V_{ao} = 0$
3	[0 0 1 1]	$V_{ao} = - V_{dc}/2$

TABLE 1: Sequences of control vectors

The inverter output voltages are written as follow

$$V_{ao} = \frac{1}{3}(V_{ab} - V_{ca})$$
$$V_{bo} = \frac{1}{3}(V_{bc} - V_{ab})$$
$$V_{co} = \frac{1}{3}(V_{ca} - V_{bc})$$

Modulation index (m_a) is defined as

$$ma = \frac{Ar}{(n-1)Ac}$$

Where Ar and Ac are the peak to peak values of V_{ao} and V_c respectively.

B. The higher level inverter control strategy

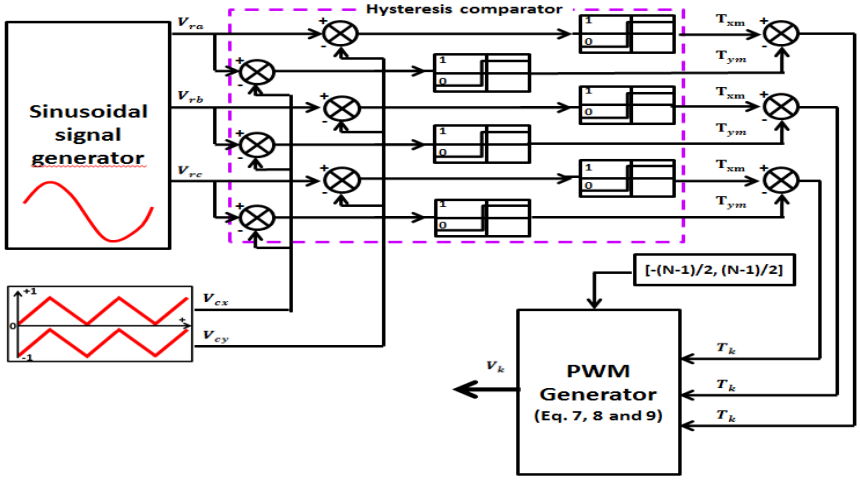

Fig. 5: Principle SPWM multilevel inverter control

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The last study for the *three-level* voltage inverter is now extended to higher level inverters. For an *n-level* inverter, it is possible to determine the number of components that are needed per arm (number of switches, diodes, carrier, etc).

Numbers of inverter components calculation :
Define S_{eq} as the number of commutation sequence possibilities. S is the number of secondary voltage sources. K stands for the number of switches per phase. D is the number of diodes loop including the diode switches per phase. C represents the magnitude of the voltage across each capacitor and P is the number of carriers.

The following equations provide how these quantities are calculated and table 2 shows the values for several multilevel inverters.

$$S = P = n - 1$$

$$S_{eq} = 2^{(n+1)}$$

$$K = 2(n-1)$$
$$D = 4n - 6$$
$$C = \frac{Vdc}{n-1}$$

n	Seq	S=P	K	D	C
3	16	2	4	6	$V_{dc}/2$
5	64	4	8	14	$V_{dc}/4$
7	256	6	12	22	$V_{dc}/6$
9	1024	8	16	30	$V_{dc}/8$
11	4096	10	20	38	$V_{dc}/10$
15	65536	14	24	54	$V_{dc}/14$

TABLE 2: Sequences of control vectors

Calculation of carrier :
A bipolar sawtooth carrier is illustrated at Figure 6. The voltages V_{cx} and V_{cy},_ have the expression given by equation as fallows:

$$V_{cx} = \sum_{x=2}^{h} V_{cx-1} + 1$$
$$V_{cy} = \sum_{y=-2}^{-h} V_{yx-1} - 1$$

Calculation of reference voltages :
The balanced three-phase reference voltage is given by :

$$Vra(t) = A_r \sin(2\pi f_r t)$$
$$Vrb(t) = A_r \sin(2\pi f_r t - \frac{2\pi}{3})$$
$$Vrc(t) = A_r \sin(2\pi f_r t - \frac{4\pi}{3})$$

where V_r is the three phase reference voltage.

Calculation of the comparator :
The comparator uses the reference and carrier signals to generate a binary signal according to the following equation :

$$\text{If } V_r \geq V_{cx} \Rightarrow T_{xm} = 1$$

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$$\text{or}$$
$$\text{If } V_r < V_{cx} \Rightarrow T_{xm} = 0$$
$$\text{and}$$
$$\text{If } V_r < V_{cy} \Rightarrow T_{ym} = 1$$
$$\text{or}$$
$$\text{If } V_r > V_{cy} \Rightarrow T_{ym} = 0$$

Calculation of the adder :

The parameter T_k is the difference between T_{xm} and T_{ym} . It is therefore calculated as follows.

$$T_k = T_{xm} - T_{ym}$$

Calculation of inverter control vectors:

The generation of the pulse vector that control the inverter is very important. The pulse vector can be generated by applying the G_n vector for each T_k according equation. The inverter output voltage V_k is given by equation as fallows :

$$\text{If } T_k = \frac{n-1}{2} - i \Rightarrow \begin{Bmatrix} G_1 = [0..0\ 1..1] \\ G_2 = [1..0\ 0..1\ ] \\ G_3 = [1..0\ 0..1] \\ \dots \\ G_n = [1..1\ 0\ ..0] \end{Bmatrix}$$

$$V_k = \frac{h - i}{n - 1} V_{dc}$$

Where $h = \frac{n-1}{2}$, $i = \{0,1,2,\dots,n-1\}$ and Gn is $1 \times 2(n-1)$ Vector .It contains $1 \times (n-1)$ Zero vector and $1 \times (n-1)$ ones Vector.

III. CASE STUDY: NINE-LEVEL INVERTER INDUCTION MACHINE CONTROL

This section presents on a case study for a nine-level inverter that is used to drive an induction machine. From equation (4), when (n = 9), the number of components required is: 8 secondary voltage sources, 16 switches per arm, 30 diodes per arm, and 8 carriers. The corresponding SPWM control pulse vectors are given at Table 3. Fig. 7 shows the reference and carrier signals. The voltages across the capacitors have the same values $V_{dc}/6$. The inverter output voltage V_k which is the voltage between phase and neutral is given at Table 3. The three phase voltages V_{ao},V_{bo} and V_{co} have the same shape but they are phase-shifted by 120°.

T_k	G_n	V_k
4	[1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0]	$\frac{4}{8}$Vdc
3	[0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0]	$\frac{3}{8}$Vdc
2	[0 0 1 1 1 1 1 1 1 1 0 0 0 0 0 0]	$\frac{2}{8}$Vdc
1	[0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 0]	$\frac{1}{8}$Vdc
0	[0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0]	0
-1	[0 0 0 0 0 1 1 1 1 1 1 1 1 0 0 0]	$-\frac{1}{8}$Vdc
-2	[0 0 0 0 0 0 1 1 1 1 1 1 1 1 0 0]	$-\frac{2}{8}$Vdc
-3	[0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0]	$-\frac{3}{8}$Vdc
-4	[0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1]	$-\frac{4}{8}$Vdc

TABLE 3 : SPWM Pulse Vector Control

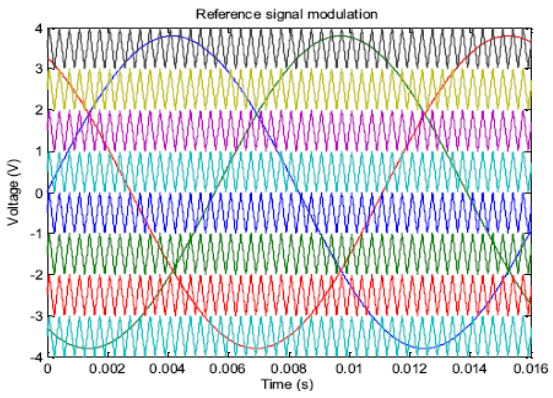

Fig. 7: Modulation signals of *nine-level* SPWM

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One can notice that SPWM voltage of the nine level output is shown in fig (8).In fig (9) shows the output voltage waveform has nine-level .

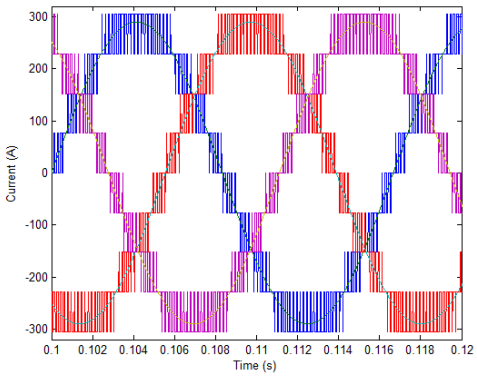

Fig. 8: SPWM voltage of nine-level output

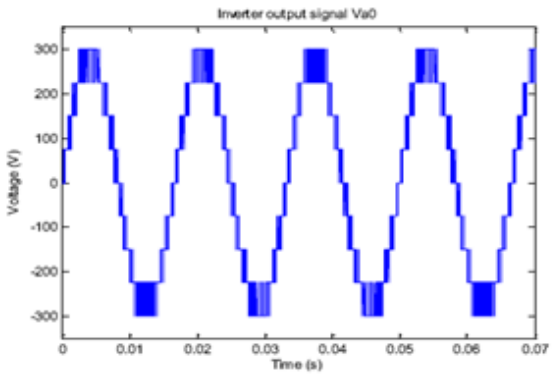

Fig 9 : Output voltage V_{ao} of nine level inverter

IV. TOTAL HARMONIC DISTORTION (THD) ANALYSIS OF MULTILEVEL INVERTER

The main criterion for assessing the quality of the voltage delivered by an inverter is the Total Harmonic Distortion (THD). This section will be devoted to analyzing the inverters performance according to their number level. Level three, nine and fifteen inverters will be considered. The main aim is to see if the low order harmonics amplitude will decrease when the number of level increases. The inverter is usually followed by a low pass filter since higher frequency harmonics are easy to filter. This means that the performance of multilevel inverters can be improved by cancelling or reducing lower order harmonics. Lower order harmonics generate the most important currents when an inductive load is used.

The THD is a measure of closeness in a shape between the output voltage waveform and its fundamental component. It is defined as the ratio of the RMS value of its total harmonic component of the output voltage and the RMS value of the fundamental component. Mathematically, THD as follows:

$$THD = \frac{\sqrt{E_{0\,rms}^2 - E_1^2}}{E_1}$$

V. SIMULATION CIRCUIT & RESULTS

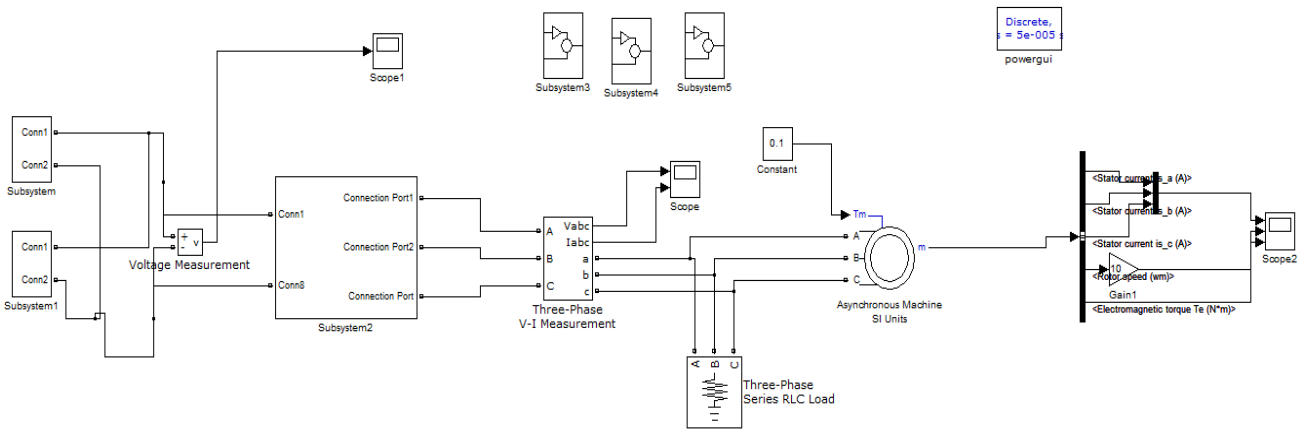

Fig: (10) MATLAB implementation of the Multilevel inverter fed an induction Motor

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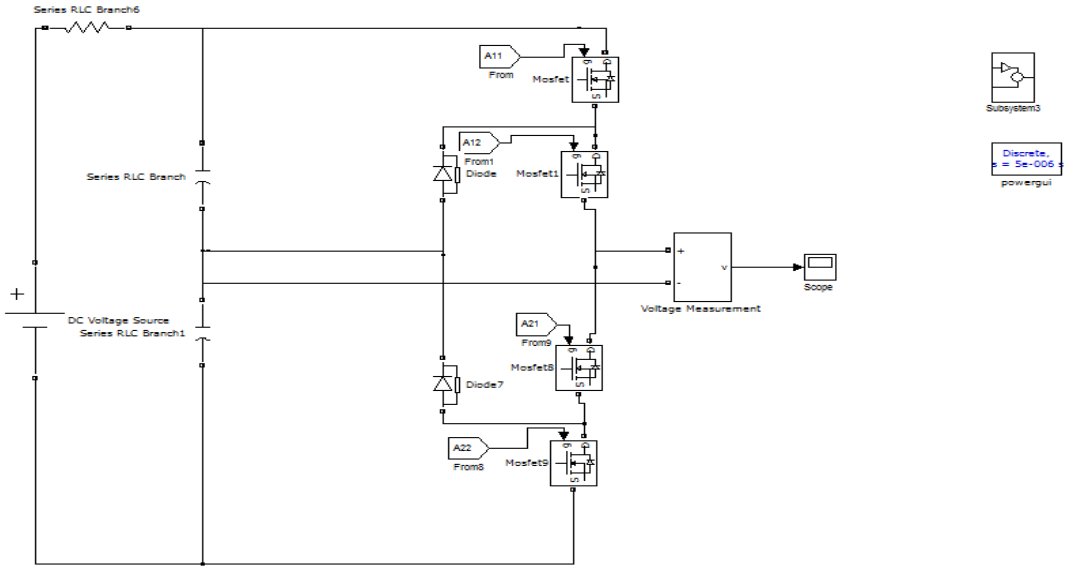

Fig (11) : Simulation diagram for a 3 level Multilevel inverter

In Fig 10 indicates that the MATLAB circuit implementation of the Multi level inverter fed an induction Motor. Fig 11 represents the Simulation diagram foe a 3 Level multilevel inverter. By using with different multilevel inverters i.e., 3,5,9 and 15 level the THD values are found form FFT analysis. Here different Multilevel inverters FFT analysis are shown in below figures.

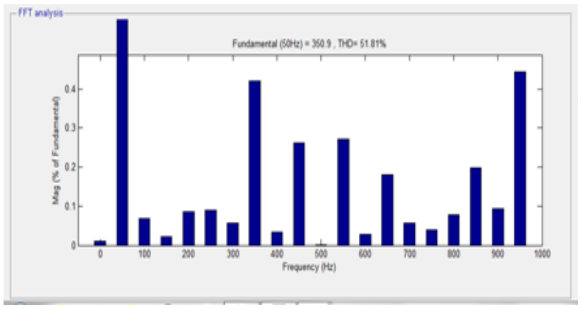

Fig 12 (a): FFT analyse of three-level inverter

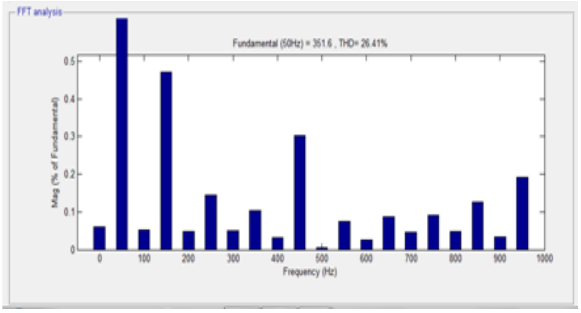

Fig 12 (b): FFT analyse of Five-level inverter

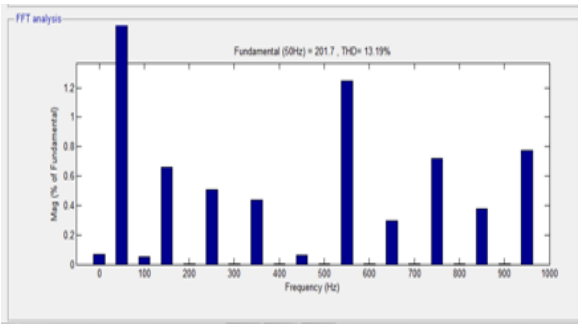

Fig 12 (c): FFT analyse of nine-level inverter

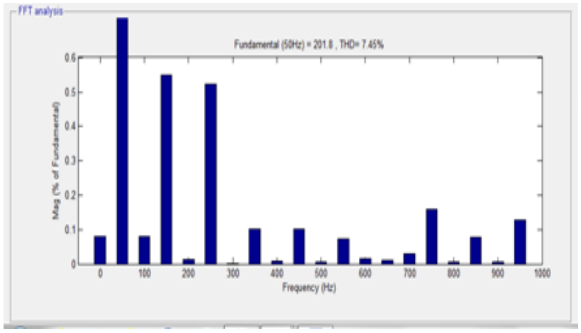

Fig 12 (d): FFT analyse of Fifteen-level inverter

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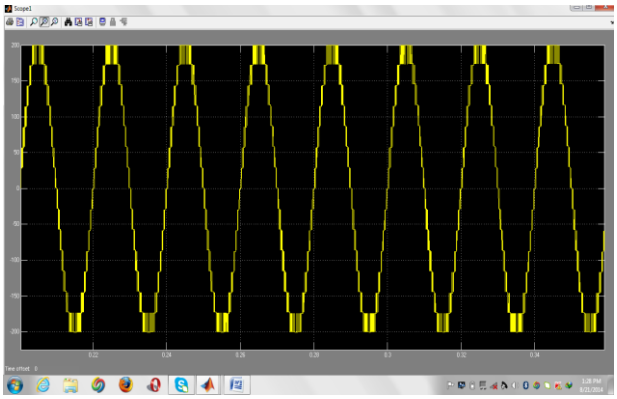

Fig 12(e) : Output Voltage for the Fifteen level inverter

S.no	Type of Multilevel inverter	THD
1	3	51.81%
2	5	26.41%
3	9	13.19%
4	15	7.45%

TABLE 4: Results Comparison

In Fig 12 (a),(b),(c) & (d) are the FFT analysis for the 3,5,9 &15 level multilevel inverters. The Output voltage of the fifteen level multi level inverter. Finally the results Comparison table will gives the various THD values for different levels of multilevel inverter is shown in TABLE 4 . This simulation demonstrates that the magnitude of the harmonics get smaller when the number of level is increased. It becomes therefore easy to remove those harmonics with a simple low-pass filter.

V. CONCLUSIONS

In this paper, a general multilevel SPWM control algorithm for n-level inverter has been modelled and simulated using Matlab/Simulink. This algorithm can generate automatically SPWM pulses for any level of inverter by changing only a parameter n which is the number of inverter level. Simulation of 3,5,9 and fifteen level inverter connected to induction motor has been performed and the generated signals THD are analysed. The system is supplied by a PV panel and batteries bank. That gives energy autonomy to the system. Simulation results give a better quality of stator current in terms of low harmonics, thus reducing the adverse effects on of the machine life and eventually the electrical network which supplies it. We have also highlighted that at fifteen-level, the harmonics are very low. These latter can be easily eliminated with a simple low-pass filter. So it is not necessary to continue increasing the inverter level.

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BIOGRAPHY

Mr.BANDI. NAGA SURENDRA pursuing M.Tech in Geethanjali Institute Of Science &Technology, Nellore, JNTU Ananthpuram. His Specialization is Power Electronics. His Research interest includes Power Electronics and Drives. He is having 4 years experience as an Electrical Site Engineer.Attended Couple of WORKSHOPS i.e.,MATLAB Workshop, Principles Of Power System Reliability and Poster Presentation.

Mr.Murali Dasari received Bachelor of Technology degree in Electrical & Electronics Engineering from MITS, JNTUH and Master's degree from VNRVJET,Hyderabad. Currently, working as an Assistant Professor in Geethanjali Institute Of Science &Technology,Nellore,JNTU Ananthpuram,A.P. He is having 6 years of teaching experience. His areas of interests in Power electronic & drives.

Mr.T.Ravi kumar received Bachelor of Technology degree in Electrical & Electronics Engineering from Narayana engineering college Nellore, JNTUH and Master's degree from JNTU college of Engineering, Anantapur . Currently, pursuing Ph.d in KL University and working as an Associate Professor in Geethanjali Institute Of Science &Technology, Nellore, JNTU Anantapur, A.P. He is having 7 years 6 months of teaching experience .His areas of interests in Power systems and Power electronic & drives. His research interests include electric machines, machine drives, power electronics/conversion, and practical use and improvement of modern control and estimation theory in electric machine drives and power electronics control.