ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

System Level Tools for Designing FIR Filter on FPGA

Mrs.Bhagyalakshmi N[1], Dr.Rekha K R[2] , Dr.Nataraj K R[3]

Research Scholar, Dept of ECE, Jain University, Bangalore, India[1].

Professor, Department of ECE, SJBIT, Bangalore, India[2].

Professor and Head, Department of ECE, SJBIT, Bangalore, India[3].

ABSTRACT: In this paper, Design of FIR Filter using System Level Tools like Simulink in Xilinx System Generator and hardware based FIR Filter Design using Verilog has been proposed. System level tools like Xilinx System Generator are used to design an efficient DSP Algorithms and Applications on FPGA. Both the designs have been further synthesized on Xilinx Spartan3 FPGA kit. Finally, a comparison is done between the results obtained from the software simulations and those from FPGA.

KEYWORDS: DSP, FIR filter, FPGA, Simulink, System Generator.

I. INTRODUCTION

Digital Signal Processing Techniques are used in many applications, mainly in communication field, video processing and multimedia.DSP algorithms requires a number of mathematical operations to be performed very quickly.DSP functions mainly contain Digital Filters and Transforms that have advantages over analog designs. Digital filters have become an increasingly attractive replacement for analog filters due to recent advances in semiconductor technology. As the speed of operation increases, either to permit real-time processing of wide-band signals or to time share the arithmetic unit, there is a rapid increase in hardware complexity, as measured by the number of IC's used, and in power consumption. The major factor causing this increase lies with the high-speed multipliers [1].

II. RELATED WORK

MATLAB based Simulink Tool helps to design the model based diagram and simulation, automated code generation and verification of corresponding design on high end FPGA's. Filter Design and Analysis (FDA) Tool is a powerful tool in MATLAB Signal Processing Tool box, with the help of which we can design and analyze different types of Filters [2].

The recent progress in software tool development is to support DSP applications widely in FPGAs. System Generator for DSP™ is the Industry's leading high-level tool for designing high-performance DSP systems using FPGAs [3].System Generator tool provides Simulink libraries to design Arithmetic, Logical, Mathematical, Memory blocks and DSP functions [4]. The DSP functions include FIR Filters and Transforms. In this paper we are designing the FIR Filters using System Generator models with the help of FDA Tools.

The designing of a Filter essentially comprises of two basic steps that completes the design process. The first step is the generation of coefficients and the second step constitutes the simulation of filter using the generated coefficients. Although FIR Filter design is complicate, the advantages persisting allows them to be widely used for filtering applications when compared to IIR Filters. IIR filters do not provide stability at higher orders whereas the FIR counterparts are always stable and are particularly useful for applications which require exact linear phase response [8].

The paper is organized as follows: Section 2 gives a Brief review of the FIR Filter design. Section 3 presents the FIR Filter Design using System Generator. Section 4 presents the results and comparison of the FIR Filter design. A conclusion is given in Section 5.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

III. FIR FILTER DESIGN

In digital design, the Finite Impulse Response (FIR) can be viewed as a functional diagram shown in the Fig 1 and implemented using the equation (1) given below [5].

$$Y[n] = \sum_{i=0}^{N-1} H[i]X[n-i] \tag{1}$$

Where N= Number of coefficients or Taps, X= input data,

Y= output data and H= filter coefficients.

The coefficients of the FIR filter are generated by using DFT of known frequency transfer function.

Fig 1: Functional Block of Digital Filter.

Here we have designed parallel implementation of 4-Tap FIR Filter as shown in the Fig 2.The filter contains mainly multiplication block, adder block, and flip-flops. The flip-flops act as registers to store the data temporarily. The input data is multiplied with filter coefficient. Results are stored in register. Next multiplied data is added with the data in the register to faster the process. Hence delay will be avoided. Due to the usage of registers glitching problem will be filtered. So it reduces the power consumption of the design.
The design is in its transposed form. This design is basic FIR Filter multiplier based design. Now a day's many multiplier less architectures are available in market.

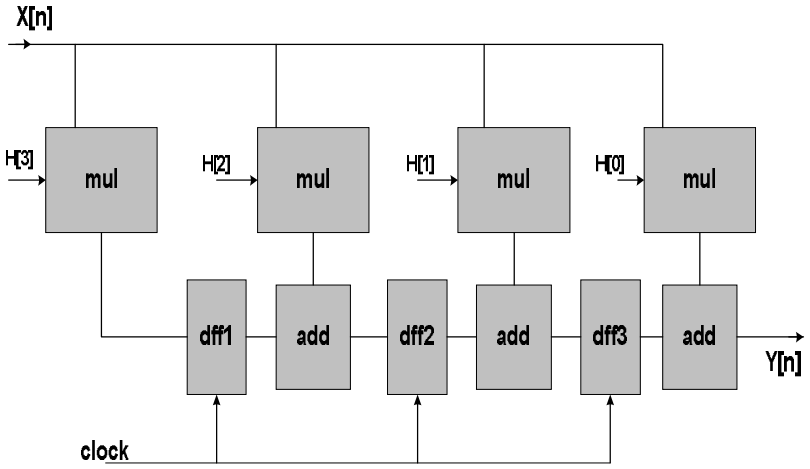

Fig 2: 4-TAP Filter Implementation

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

IV. FIR FILTER DESIGN USING SYSTEM GENERTOR

System generator is a high level system design tool for creating custom DSP blocks on FPGA easily. System generator basically provides two key tools:

- Blocks for building the model.
- Hardware generator model.

Simulink provides a test environment for the design [9].

Fig 3 shows the 3-Tap Filter design. The input is a Chirp signal which gives the up frequency or down frequency with time and Output signal is a linear Chirp signal (sine wave whose frequency varies linearly with time).

The design is a Low Power 3-Tap FIR Filter design using Least Square method as shown in the Fig 3. Least mean square (LMS) algorithm is used in adaptive filters to find the filter Coefficients that relate to producing the least mean squares of the error signal (difference between the desired and the actual signal).

It is one of the optimal filter design methods for designing an FIR Filter. The basic idea is to generate the filter coefficients again and again until a particular error is minimized. The purpose of most of the filters is to separate the desired signal from undesired signal or noise. As the energy of the signal is related to square of the signal, a squared error approximation criterion is appropriate to optimize the design if FIR filters. The choice of LMS algorithm lies in its simplicity of implementation, Stable and robust performance against different signal conditions.

The input signal frequency is 100MHZ and the Frequency specifications of Filter are as follows:

Fs=48000 Hz, Fpass=9600Hz, Fstop=12000Hz.

The coeffiecients are generated by using FDA tool. We have to export the coeffiecient values to MATLAB workspace and save as a variable name Num. Num contains 4 coeffiecients as given below.

coeffiecient1= 0.180209484969501
coeffiecient2= 0.407209809882283
coeffiecient3= 0.407209809882283
coeffiecient4= 0.180209484969501

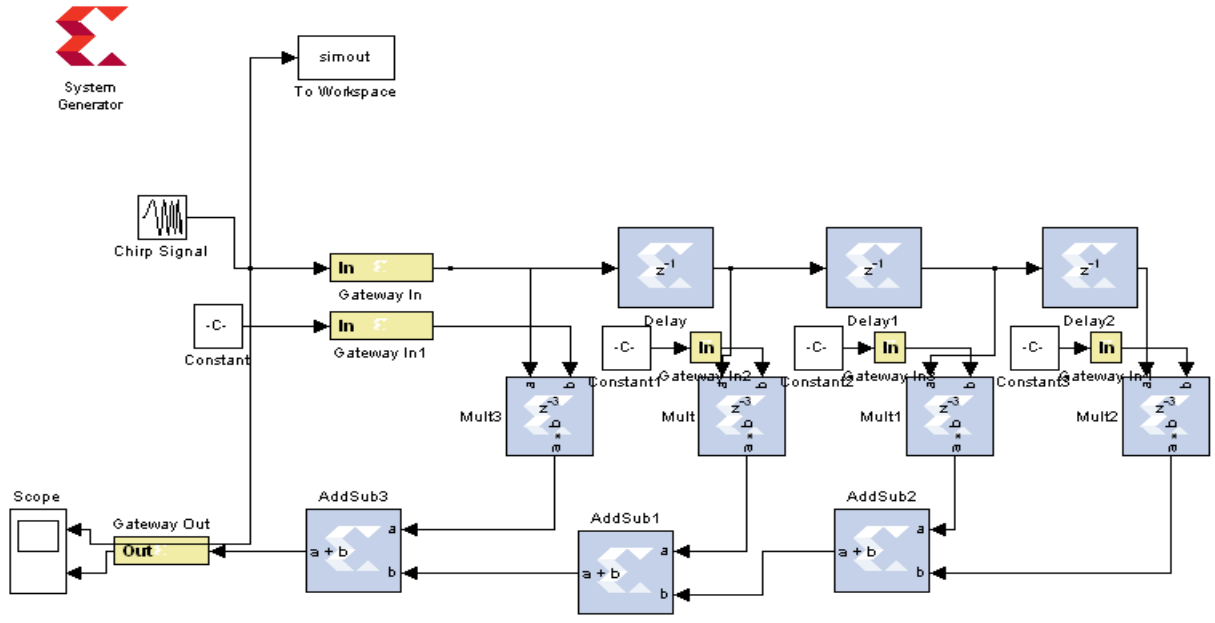

Fig 3: 3-Tap FIR Filter Design Using System Generator

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

The magnitude (100db) and frequency plot is as shown in Fig 4.

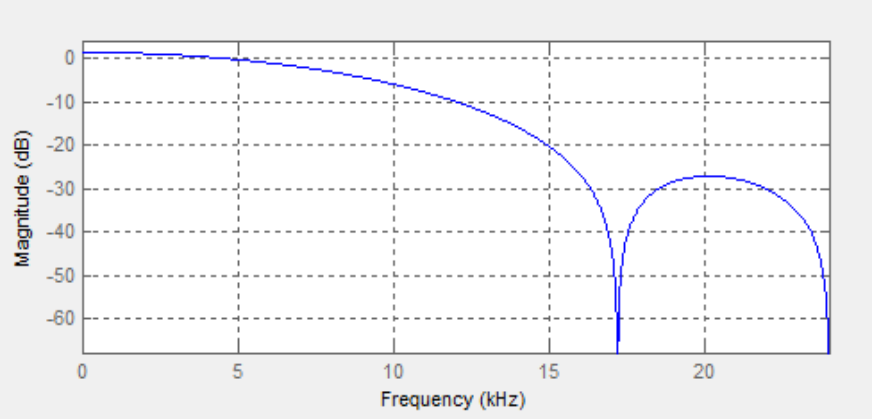

Fig 4: Magnitude (100db) v/s Frequency Plot.

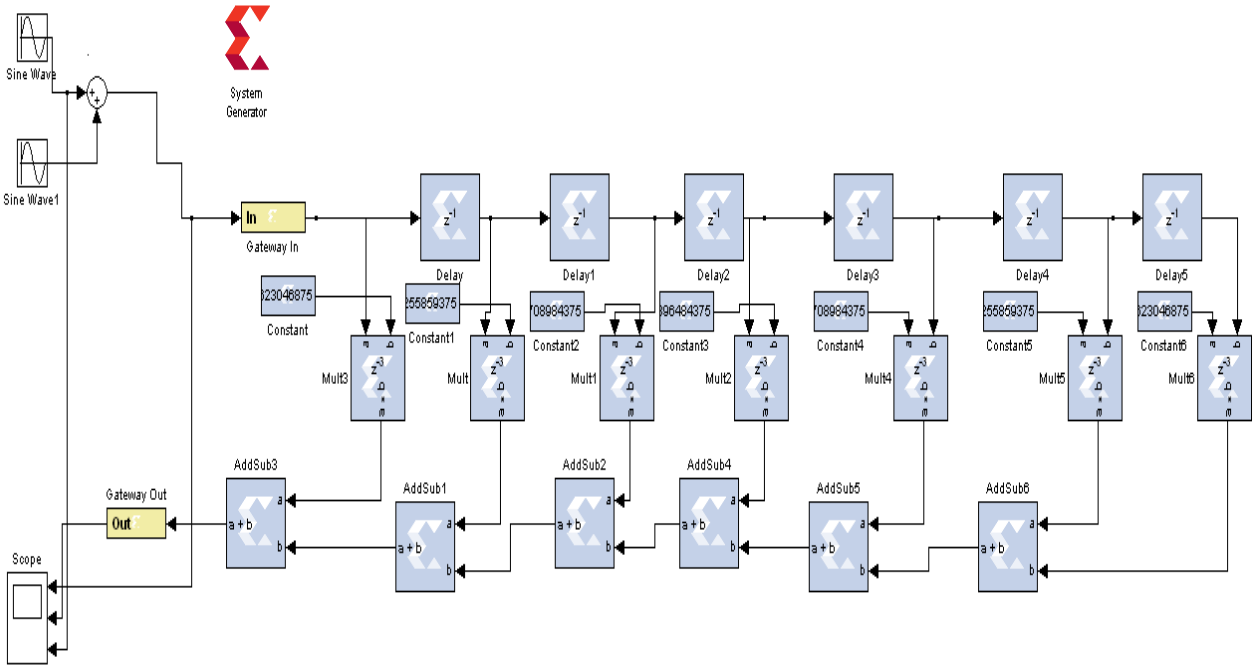

Fig 5: 6-Tap FIR Filter Design Using System Generator For Different Input Frequencies.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

The Fig 5 shows the 6-Tap Filter design using 2 different input frequencies. The input signal is a sine wave with 2 different frequencies.The coeffiecients are generated by using FDA tool. It contains 7 coeffiecients.

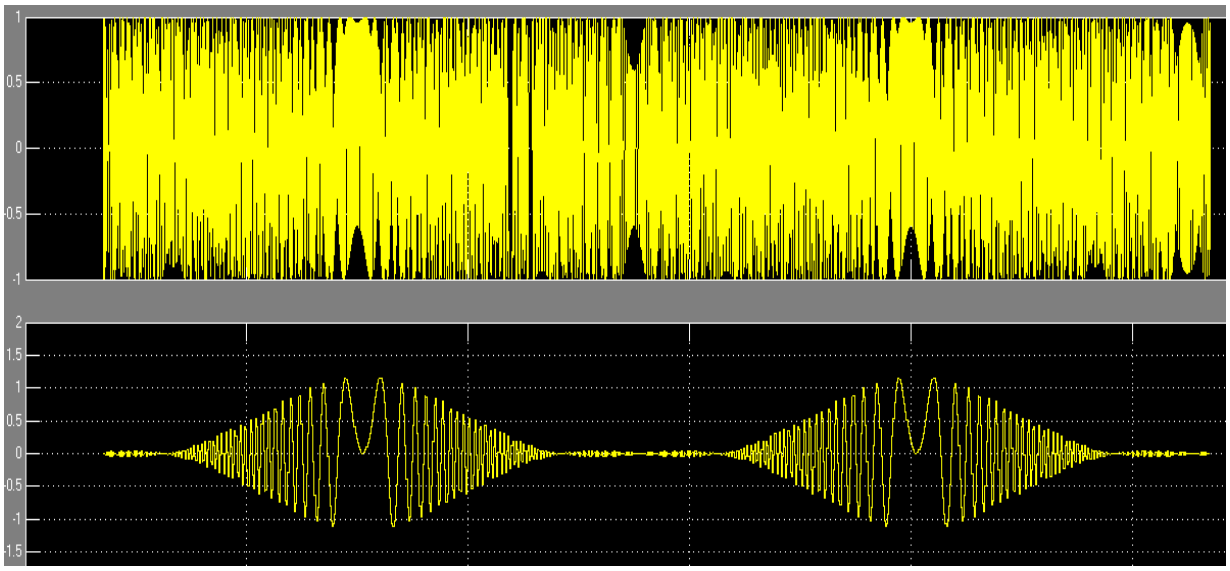

Fig 6: Simulink Simulation Results for 3-Tap Filter.

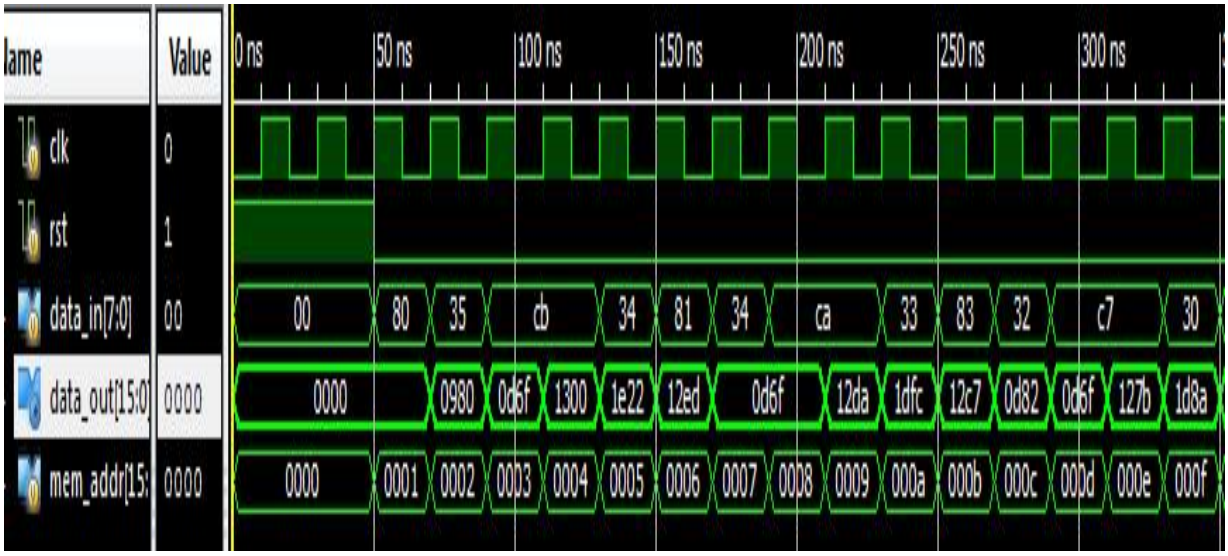

Fig 7: Simulation Results For Hardware Based 3-Tap FIR Filter.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

V.RESULTS AND COMPARISON

The Simulink Simulation results for 3-Tap Filter using System Generator is shown in the Fig 6. It contains Chirp signal as an input (above) and filtered output (below) in Fig 6.
The Verilog based 3-Tap FIR Filter Simulation results are as shown in the Fig 7.The input for hardware based 3-tap FIR filter is a Chirp signal which is generated with the help of simout as shown in Fig 3 in text form to FIR design .Then simulated using I-sim simulator.

Comparision for System Generator based and Hardware based FIR Filter module is as given below.

Table I: Comparision of FIR Filter Module.

	System Generator design		Verilog based design		
Logic Utilization	**Used**	**utilization**	**Used**	**utilization**	**Available**
Number of Slices	49	1%	14	0%	3584
Number of Slice Flip Flops	96	1%	27	0%	7168
Number of bonded IOBs	56	39%	26	18%	141
Number of GCLKs	1	12%	1	12%	8

VI.CONCLUSION

This paper describes a System Level approach towards the implementation of FIR Filters using System Generator and subsequent Verilog synthesis on Field Programmable Gate Arrays (FPGA). The parallel implementation of FIR Filter is excellent in terms of area and System Generator model greatly increases the speed of operation in the implementation of the FIR Filter. With the help of System Level tools we can design any DSP model in short time and is suitable for high speed FPGA's.

REFERENCES

[1] A. Peled and B. Liu, "A new hardware realization of digital filters", IEEE Transactions on A.S.S.P., vol. ASSP-22, pp. 456–462, December 1974.
[2] MathWorks→products→Simulink, http://www.mathworks.com/products/simulink/.
[3] Xilinx system generator, DSP user guide, www.xilinx.com.
[4] James Hwang and Jonathan Ballagh, "Building Custom FIR Filters Using System Generator", Xilinx Inc. 2100 Logic Drive, San Jose, CA 95124 (USA).

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 2, February 2014

[5] Fábio Fabian Daitx, Vagner S. Rosa, "VHDL Generation of Optimized FIR Filters",International Conference on Signals, Circuits and Systems, 2008.
[6] Oppenheim, A. V. and R. W. Schafe , "Discrete-Time Signal Processing", Englewood Cliffs, NJ: Prentice Hall, 1989.
[7] Proakis, J. and D. Manolakis, "Digital Signal Processing", 3rd ed. Englewood Cliffs, NJ: Prentice-Hall, 1996.
[8] Ritu Saroha, Surender Dhiman, "Designing and Comparison of FIR Filter using Xilinx System Generator", International Journal of Advanced and Innovative Research (IJAIR), vol.2, no.8, pp.207-210, 2013.
[9] Evan Everett and Michael Wu, "Introduction to Xilinx system generator", ELEC 433-Spring 2013.

BIOGRAPHY

Mrs. Bhagyalakshmi. N obtained her M.Tech Degree from Visvesvararaya Technological University, Bangalore,India in 2007. She is pursuing her PhD degree in Jain University, Bangalore, India. Presently she is working as Assistant Professor in the department of Electronics and Communication Engineering at Vivekananda Institute of Technology, Bangalore. Her research interests include FPGA Implementation,VLSIDesign and Embedded Systems.Received Best Base paper award for the Conference paper titled"Analysis of High Performance FIR Filter Using Improved Distributed Arithmetic",Oct 2013.

Dr. K. R. Rekha obtained her PhD degree from Dr.MGR University, Chennai, India in 2011. Presently She is working as Professor in the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. Her research interests include Wireless communication, FPGA implementation, Microcontroller and Embedded Systems Design. She is a member of MIE, MISTE and IETE.

Dr. K.R.Nataraj obtained his PhD degree from Dr.MGR University, Chennai, India in 2010. He worked as Professor and Head of the Department during 2000-2008 and as Post Graduate Coordinator in the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. Presently, He is heading the Department of Electronics and Communication in SJB Institute of Technology, Bangalore. His research interests include Wireless communication, FPGA implementation, and Microcontroller and Embedded systems design. He is a member of MIE, MISTE, IETE and IEEE.